MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

②

AD-A161 611
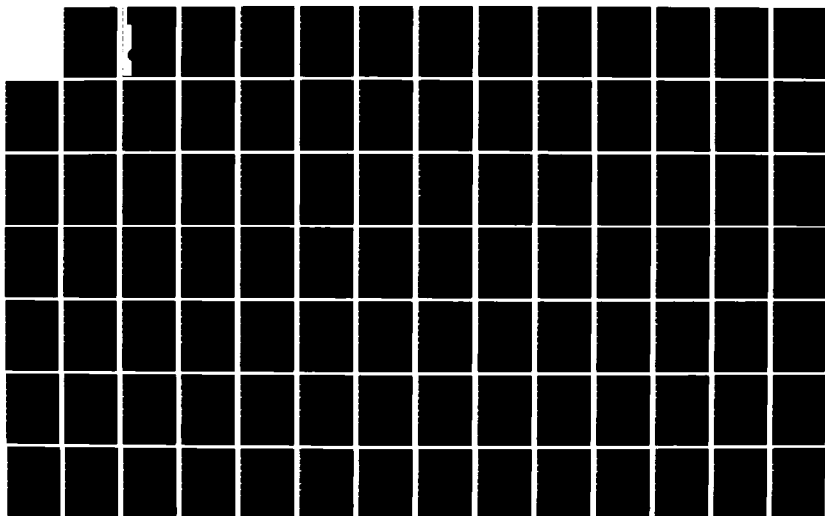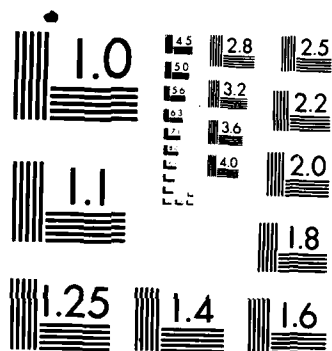
HARMONIC POWER GENERATION OF IMPATT DIODES

FINAL REPORT

September 1985

By

C. K. PAO

DTIC
ELECTE
NOV 2 5 1985
S D

B

SOLID STATE ELECTRONICS LABORATORY

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE THE UNIVERSITY OF MICHIGAN, ANN ARBOR

11 19-85 049

THE VIEWS, OPINIONS, AND/OR FINDINGS CONTAINED IN THIS REPORT ARE
THOSE OF THE AUTHOR(S) AND SHOULD NOT BE CONSTRUED AS AN OFFICIAL
DEPARTMENT OF THE ARMY POSITION, POLICY, OR DECISION, UNLESS SO
DESIGNATED BY OTHER DOCUMENTATION.

HARMONIC POWER GENERATION OF IMPATT DIODES

by

C. K. Pao

Final Report

Solid-State Electronics Laboratory
Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, MI 48109-1109

Approved for public release; distribution unlimited.

September 1985

ABSTRACT

The harmonic power generation capability of IMPATT diodes is investigated theoretically and experimentally. The existing computer simulation program for IMPATT diodes, employing the drift-diffusion model, is used to investigate four different conventional double-drift IMPATT diodes operated in the active mode and three pin diodes with different lengths operated in the passive mode at a fundamental frequency of 23 GHz. For conventional IMPATT diodes, the depletion-layer modulation effect, which strongly depends on the diode doping structure, is essential for harmonic power generation. Because of the moderate dependence of the harmonic current on the terminal RF voltage, and GaAs and Si uniform diodes seem to be promising devices for harmonic power generation. The GaAs uniform diode can achieve the highest third-harmonic efficiency, of the order of 4.1 percent, while the Si uniform diode can achieve the highest third-harmonic power of the order of 1.116 W.

In the case of pin diode structures, the device length determines the device RF power performance since it determines the space-charge and transit-time effects, both of which in turn affect the build-up and fall-off of the induced current. The optimum device length for achieving the highest third-harmonic power is approximately 0.827 μm. However, over 100-percent conversion of efficiency from the fundamental input power to the third-harmonic output power can be achieved.

An analytic model for three-frequency operation, without considering the depletion-layer modulation effect, was developed to investigate the GaAs double-Read diode. The calculated results showed that the third-harmonic power is low and the presence of the diode series resistance significantly decreases it.

Several waveguide circuits were designed for measurement of the RF power of GaAs double-Read diodes and Si single-drift uniform diodes. The best measured RF power levels for the GaAs diodes are 175 mW at 22.58 GHz, 2 mW at 45.59 GHz and 17 μW at 67.69 GHz, and those for the Si diodes are 15 mW at 32.43 GHz, 0.17 mW at 64.95 GHz and 2.2 μW at the third-harmonic frequency.

Acce

By
Distr

Availability Codes

| Dist | Avail and/or Special |

A-1

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF SYMBOLS

A	Device area.
A	Quantity defined in Fig. 1.4.
A,B	Coefficients appearing in Eq. 2.73.
a,b	Waveguide width and height.
a_k, b_k	Coefficients in Eqs. 3.51 and 3.52.
b_n, A_n, b_p, A_p	Coefficients appearing in the hole and electron ionization rate.
C,C(V)	Depletion-layer capacitance.
C_a, C_d	Avalanche and drift region capacitances.
C_p	Parasitic capacitance.
c,l	Distance between the waveguide post and the side wall.
D	Diameter of the diode.
D_n, D_p	Electron and hole diffusion coefficients.
D_{no}, D_{nsat}, E_d	Coefficients appearing in electron diffusion expression in GaAs.
E	Electric field.
$\tilde{E}$	Small ac component of E.
E_c	Electric field intensity at the metallurgical junction.
EFF_{13}	Conversion efficiency from the fundamental to third harmonic.
EFF_n	Dc to RF conversion efficiency at frequency $n\omega$.
Eff'_{13}	Defined by Eq. 2.65.
E_v	Critical electric field corresponding to peak electron.
f_1, f_2, f_3	Fundamental, second- and third-harmonic frequencies, respectively.
f_c	Cutoff frequency of the waveguide for the TE mode.
f_ω	Useful frequency band of the waveguide.

G	Generation rate.
G_{d_m}, B_{d_m}	Device conductance and susceptance at the frequency $m\omega$.
H	Magnetic field.
I_{inj}, I_{ind}	Injected and induced current, respectively.
I_{max}	Maximum induced current.
I_n	Phasor component of the induced current at $n\omega$.
$I_n(v)$	Modified Bessel function of the first kind.
I_p	Pulsed current amplitude.
I_s	Dc current at the start-oscillation condition.
J_c	Conduction current.
J_{co}	Coefficient used in Eq. 3.1.
J_{dc}	Dc current density.
J_{dcs}	Dc current density at the start oscillation condition.
J_{indm}	Maximum induced current density.
J_{inj}, J_{ind}	Injected and induced current density, respectively.
J_{injm}	Maximum injected current density.
$\tilde{J}_{inj}^m$	Injected current phasor at the frequency $m\omega$.
J_m	Induced current phasor amplitude at the frequency $m\omega$.
J_{mN}	Normalized J_m.
J_n, J_p	Electron and hole current densities.
$\tilde{J}_n, \tilde{J}_p, \tilde{J}_t$	Small ac components of J_n, J_p and J_t.
J_{nd}, J_{pd}	Spatial distributions of electron and hole currents in the drift region, respectively.
J_s	Saturated current density.
J_t	Total terminal RF current density.
J_{tm}	Phasor component of J_t at the frequency $m\omega$.
k	Wave number for TE_{10} mode.
k, m, n	Harmonic numbers.

k_1, k_2	Thermal conductivities of buffer and active layers.
k_d	Diffusion constant for electrons and holes in Si.
k_{GaAs}, k_{Si}	Thermal conductivities of GaAs and Si.
k_g, k_t, k_p	Thermal conductivities of gold, titanium and platinum, respectively.
k_{hs}	Thermal conductivities of the heat sink.
L_m	Circuit inductance at the frequency $m\omega$.
l_d	Drift region length.
M	Multiplication factor.
M_A, M_B	Matrices defined in Chapter III.
N	Doping concentration at the depletion-layer edge.
N_B	Background doping concentration.
N_D, N_A	Donor and acceptor concentrations, respectively.
N_{eff}	Effective doping concentration.
n, p	Electron and hole concentrations, respectively.
P_1, P_2, P_3	Fundamental, second- and third-harmonic power, respectively.
P_1', P_3'	Input fundamental and output third-harmonic power shown in Fig. 2.58.
P_{3out}	Defined by Eq. 2.69.
P_m, P_n	Output power at the frequencies $m\omega$ and $n\omega$.
p, q, r	Indices used in Eqs. 3.62.
q	Magnitude of electronic charge 1.602×10^{-19} C.
R_{cm}, X_{cm}	Real and imaginary parts of Z_{cm}, respectively.
R_{in}	Input resistance seen from the coaxial line to the waveguide.
R_m, K_m	Real and imaginary parts of $[(\beta_m/v_{am}) - m^2 X/\rho_m)]$.
R_{mo}, K_{mo}	Values of R_m and K_m at the operating point, respectively.
R_t, X_t	Real and imaginary parts of the total impedance, respectively.

R_{th}	Thermal resistance.
T	Temperature.
t	Time.
t_1, t_2	Thickness of the buffer and active regions, respectively.
t_g, t_p, t_t	Thickness of gold, platinum and titanium layers, respectively.
V_{31}	Ratio of V_3 to V_1.
V_a, V_d	RF voltage across the avalanche and drift regions, respectively.
V_{am}, V_{dm}	Phasor magnitudes of V_a and V_d at frequency $m\omega$, respectively.
V_{bb}	Back-bias voltage.
V_{dc}	Dc voltage.
V_{inp}	Value of V_{in} at the maximum EFF_1 point.
V_m	Phasor amplitude of terminal RF voltage at frequency $m\omega$.
V_{mN}	Normalized V_m.
V_{RF}	RF voltage.
V_t	Terminal RF voltage.
V_{tN}	Normalized terminal voltage.
v_{am}	Normalized phasor of V_a at frequency $m\omega$.
v_{dmax}	Maximum carrier drift velocity.
v_n, v_p	Electron and hole velocities, respectively.
v_s	Saturated velocity.
w	Total depletion-layer width.
w_n	Undepleted region edge.
w_{opt}	Optimum device length of the pin diode.
X	$(\omega_1/\omega_a)^2$.
X_s	Value of X at J_{dcs}.

x	Distance.
x_a	Avalanche region length.
x_n, x_p	Depletion layer in the n and p sides, respectively.
Z_{cm}, Z_{dm}	Circuit and device impedances at frequency $m\omega$.
Z'_{dm}	Defined in Eq. 3.13.
Z_{tn}	Total impedance at frequency $m\omega$.
Z_w	Waveguide impedance at the TE_{10} mode.
α	Impact ionization rates of the heat sink.
α'	Derivative of ionization rate with respect to electric field.
α''	Second derivative of ionization rate with respect to electric field.
α_o	Impact ionization rate at dc electric field.
α_n, α_p	Impact ionization rates for electrons and holes, respectively.
β	Wave number of TEM mode.
β_m	Normalized injected current phasor at frequency $m\omega$.
γ	Coefficient defined in Eq. 3.59.
$\delta V_{ak}, \delta\omega_k, \delta\phi_k$	Small perturbations of V_{ak}, ω_k and ϕ_k.
$\delta\bar{V}_{ak}$	$\delta V_{ak}/V_{ak}$.
ϵ	Dielectric constant.
ϵ_o, μ_o	Permittivity and permeability of vacuum, respectively.
θ_o	Defined in Fig. 1.3.
θ_a	Quantity defined in Fig. 1.4.
θ_a, θ_d	Transit angles for avalanche and drift regions, respectively.
θ_c, θ_m	Central and maximum positions of injected current.
θ_L, θ_R	Distance measured from the peak position to the left and right half-amplitude points of current, respectively.

θ_m	Phase angles of phasors of J_m and V_m at frequency $m\omega$ measured with reference to the fundamental voltage phasor.
θ_p	Peak position of induced and injected currents.
θ_ω	Half-width of injected and induced currents.
μ_n, μ_p	Low-field electron and hole mobilities, respectively.
ρ_m	Defined in Eq. 3.5.
σ	$\theta_\omega/2.36$.
τ_l	Defined in Eq. 2.31.
τ_a, τ_d	Transit angles for avalanche and drift regions, respectively.
ϕ_k, ϕ_m	Phase angles of phasor of V_a at frequencies $k\omega$, $m\omega$.
ω_a	Avalanche resonant frequency.
ω_k, ω_m	Kth and mth harmonic frequencies.

CHAPTER I

INTRODUCTION

1.1 Historical Background

An IMPATT diode is a solid-state device that employs avalanche breakdown and transit-time effects to produce a negative resistance at microwave frequencies and above. The concept of transit-time negative resistance was first introduced by Shockley[1] in 1954. He demonstrated that the transit-time effect could produce a negative resistance in a pnp structure and such a device was successfully fabricated[2] in 1971. The IMPATT diode was proposed by Read[3] in 1958. The diode Read proposed required a narrow highly doped region followed by a low-doped region. The prescribed doping profile was beyond the state of the art of silicon (Si) technology at that time; the initial results for fabricating IMPATT diodes was disappointing. In 1965, a Si-IMPATT diode having a simple p-n junction was successfully fabricated by Johnston et al.[4] and it demonstrated RF power generation at microwave frequencies.

Since 1965, progress in IMPATT diodes has been rapid. The progress achieved is ma..ly due to the improvement in heat sink design, advances in fabrication technology, and development of theoretical models. The important improvement in heat sink design is due to the use of diamond[5] as a heat sink and the use of an integrated heat sink.[6] Both heat sink designs permitted high CW powers to be achieved. The recent advance in fabrication technology, such as the use of MBE,[7] has made it possible to realize various

-1-

doping profiles for both GaAs and Si diodes. Therefore, diodes can
be optimally designed for maximum power generation and efficiency.
The development of theoretical models (simplified and numerical)
has made a significant contribution to the understanding of the
behavior of the diodes and has provided important information for
diode design. Simplified modeling[8-11] (modifying Read's original
work) has successfully included the effects of drift-region space
charge, unequal field-dependent ionization rates, and velocities.
Despite the assumptions adopted, it provides a good description of
device behavior. Numerical modeling of these devices[12,13] has become
an effective method in understanding the behavior of diodes under
various conditions and in achieving the optimum diode design.
Recently, numerical modeling has been extended to include relaxation
time effects,[14] which play an important role in millimeter-wave diodes.
Due to thermal and electronic limitations,[15] IMPATT diodes show a
frequency dependence in output power. The output power drops quickly
as the frequency increases. However, since GaAs IMPATT diodes have
lower noise levels than Si-IMPATT diodes and yield better efficiencies,
a great deal of effort has been expended recently to improve their
performance at millimeter-wave frequencies. Recently, GaAs
modified-Read profile IMPATT diodes have been studied extensively[16-18]
and very good results at frequencies up to 60 GHz have been achieved.

   An IMPATT diode is inherently a nonlinear inductive device
due to the avalanche process. When the diode is employed in an
oscillator, harmonics will be generated. These harmonics can interact
with the fundamental signal and influence the performance of the
diode at the fundamental frequency. The influence of harmonics was

observed both experimentally and theoretically by many researchers
such as Swan,[19] Blue[20] and Schroeder and Haddad.[21] They concluded that
the presence of harmonics can modify the phase relationship between the
fundamental voltage and current; therefore, the fundamental efficiency
can be improved if the waveforms of the harmonics are appropriate. To
understand these harmonic effects, Kuvås and Lee,[22] Mouthaan[23,24] and
Brackett[25] separately established analytical models for two-frequency
operation and tried to determine the criteria for stable oscillation.
Mouthaan,[24] however, considered the possible harmonic power generation
from diodes under two-frequency operation. His model can provide
insight into the interaction between the device and circuit. Since
then harmonic effects and related power generation from diodes have
not received too much attention even though diodes are frequently
employed for the purpose of frequency conversion. This is partly
because (1) diodes can still provide reasonable amounts of fundamen-
tal power at desired frequencies and (2) complex circuits are required
for harmonic power generation from diodes. However, due to the
frequency dependence in device performance, harmonic power generation
may become an alternative way to generate RF power as the desired
frequency increases.

The power combining technique is often adopted in IMPATT
oscillators for providing higher output power. Since the first
IMPATT combiner at X-band was successfully designed by Kurokawa[26]
in 1971, various IMPATT combiners have been proposed and designed
for efficiently combining the fundamental power from several IMPATT
diodes. In 1982, a harmonic power combiner[27] was proposed. This
combiner, by utilizing a symmetric circuit, can combine the desired

harmonic power from devices and extend the operating frequency range of devices by a harmonic number n. This scheme can ease fabrication difficulties for millimeter-wave IMPATT diodes because only low-frequency diodes are needed for power generation at a high frequency. However, the diodes used in this combiner are required to be capable of generating sufficient harmonic power and providing reasonable impedance levels at the desired frequencies for matching. In addition, a symmetric circuit is required for effectively combining the harmonic powers from diodes. The latter requirement can be achieved by integrated circuit technology. A detailed investigation is carried out here to determine the potential and capabilities of harmonic power generation in these devices.

1.2 State of the Art of IMPATT Diodes

The performance of IMPATT diodes is limited by several factors, such as semiconductor material properties, series resistance, package parasitics, heat sink design, fabrication technique, and doping structure. Other limitations on device performance are related to designing a circuit for optimum performance. Since device-circuit interaction is quite complicated due to the nonlinearity of an IMPATT diode, harmonic effects may not be completely ignored in determining the optimal matching circuit. However, it is not easy to find such optimal matching circuits.

Progress has been made recently in GaAs IMPATT diodes for CW operation and Si IMPATT diodes for pulsed operation. The best experimental results reported in the literature[5,16-19,28-65] for both Si and GaAs IMPATT diodes are listed in Tables 1.1 and 1.2 and plotted

Table 1.1

State of the Art of Si IMPATT Diodes

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
8.5	6.8 W	11.8	CW	DD	1	Seidel et al.[28]
8.9	6 W	12.2	CW	DD	1	Seidel et al.[28]
10	1.7 W	10	CW	DD	1	Ying[29]
11.5	2.8 W	13.2	CW	DD	1	Pfund et al.[30]
12	7 W	12	CW	DD	1	Seidel and Niehaus[31]
13.3	4.7 W	8	CW	SD	1	Swan[5]
40.1	2.26 W	10.6	CW	DD	1	Midford and Bernick[32]
50	1 W	14.2	CW	DD	1	Seidel et al.[33]
55	1.6 W	11.5	CW	DD	1	Hirachi et al.[34]
60.5	1.2 W	0	CW	DD	1	Midford and Bernick[32]
68	0.5 W	8.7	CW	DD	1	Leistner[35]
70	0.35 W	9.2	CW	DD	1	Howard et al.[36]

*SD denotes a single-drift structure and DD denotes a double-drift structure.

(Cont.)

Table 1.1 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
77.7	1.014 W	8.1	CW	DD	1	Ino et al.[37]
86	0.32 W	12	CW	DD	1	Gokgor et al.[38]
91.9	0.98 W	3.6	CW	DD	1	Midford and Bernick[32]
95	0.22 W	10	CW	DD	1	Gokgor et al.[38]
132	86 mW	7.6	CW	SD	1	Gokgor et al.[38]
140	110 mW	2	CW	SD	1	Chang et al.[39]
170	60 mW	2	CW	SD	1	Chang et al.[39]
185	78 mW	2.3	CW	SD	1	Ino et al.[40]
202	50 mW	1.3	CW	SD	1	Ishibashi and Ohmori[41]
220	50 mW	1	CW	DD	1	Midford and Bernick[32]
228	33 mW	0.8	CW	DD	1	Midford and Bernick[32]
285	> 0.5 mW	0.35	CW	SD	1	Ino et al.[40]
295	4.5 mW	0.13	CW	SD	1	Ishibashi et al.[42]
301	1.2 mW	--	CW	SD	1	Ishibashi and Ohmori[41]

(Cont.)

Table 1.1 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
412	2.2 mW	0.47	CW	SD	1	Ishibashi et al.[42]
8	28 W	4	1 μs 0.1%	SD	1	Gilden and Moroney[43]
9.7	45 W	10	1 μs 10%	DD	1	Pfund and Curby[44]
10.2	54 W	13	1 μs 10%	DD	1	Nagao et al.[45]
16.5	11 W	12	0.8 μs 25%	DD	1	Pfund et al.[46]
35	31 W	6.5	0.1 μs 1%	DD	1	Walker and Hing[47]
65	5.3 W	5	0.1 μs 0.5%	DD	1	Freyer et al.[48]
94	13 W	8	0.1 μs 0.5%	DD	1	Chang et al.[49]
140	3 W	6	0.1 μs 0.25%	SD	1	Chang et al.[39]
170	1.3 W	2.5	0.1 μs 0.25%	SD	1	Chang et al.[39]
2.7	0.7 W	2	0.1 μs 0.25%	SD	1	Chang et al.[39]

Table 1.2

State of the Art of GaAs IMPATT Diodes

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
5	11 W	22.4	CW	SD	4	Adlerstein et al.[50]
5.7	11 W	21	CW	SD	4	Nishitani et al.[51]
6.1	15 W	25	CW	Lo-Hi-Lo	1	Hirachi et al.[52]
7.75	10 W	16	CW	DD-Read	4	Wallace et al.[53]
8.15	8 W	35.5	CW	Lo-Hi-Lo	-	Kim and Matthei[54]
9.6	5.8 W	28	CW	Lo-Hi-Lo	-	Kim and Matthei[54]
10.5	4 W	30	CW	Lo-Hi-Lo	-	Kim and Matthei[54]
11.1	5.3 W	24	CW	Lo-Hi	4	Grierson et al.[55]
13.75	3.2 W	20.7	CW	Read-S	4	Kim et al.[56]
19.6	3.1 W	18.6	CW	SD-Read	4	Berenz et al.[57]
20	4 W	21	CW	DD-Read	4	Adlerstein et al.[16]

*SD denotes a single-drift structure and DD denotes a double-drift structure. Read denotes a Read-type doping profile and S denotes a Schottky-barrier diode.

(Cont.)

Table 1.2 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode		Structure*	No. of Diodes in the Package	Reference
20.3	2.7 W	18	CW		SD-Read	4	Berenz et al.[57]
33	3 W	22	CW		DD-Read	1	Adlerstein and Moore[17]
44.1	2.1 W	19	CW		DD-Read	1	Adlerstein and Chu[18]
51.7	1.025 W	10.5	CW		DD	1	Ma et al.[58]
53	0.7 W	11.2	CW		SD	1	Zhang and Freyer[59]
60	1.24 W	11.4	CW		DD-Read	1	Adlerstein and Chu[18]
150	3 mW	0.5	CW		TUNNETT	1	Elta et al.[60]
8.3	35 W	20	1 μs	25%	DD	2	Berenz et al.[61]
8.5	31 W	23	0.3 μs	30%	DD-Read	4	Wallace et al.[53]
8.6	30 W	23	0.5 μs	10%	SD-Read	1	Hierl et al.[62]
9.3	30 W	17	1 μs	10%	DD-Read	1	Berenz et al.[61]
13	20.5 W	21	0.5 μs	10%	SD-Read	1	Hierl et al.[62]
15.4	15 W	18	0.5 μs	10%	SD-Read	1	Hierl et al.[62]
96	1 mW	--	Pulsed		SD	1	Schawarz and Bonek[63]

(Cont.)

Table 1.2 (Cont.)

Frequency (GHz)	Power Output	Efficiency (Percent)	Mode	Structure*	No. of Diodes in the Package	Reference
200	1 mW	--	Pulsed	TUNNETT	1	Nishizawa et al.[64]
338	10 mW	--	Pulsed	TUNNETT	1	Nishizawa et al.[65]

in Figs. 1.1 and 1.2. The thermal limitations (1/f slope) and
electronic limitations ($1/f^2$ slope) are also indicated in both figures.

For Si IMPATT diodes, a significant amount of power in pulsed
operation has been achieved for frequencies up to 200 GHz. Output
powers over 50 mW in CW operation for frequencies throughout the
100 to 200 GHz range have been reported. The power output data of
Si devices for both CW and pulsed operations closely follow 1/f and
$1/f^2$ slopes. Transition for 1/f to $1/f^2$ occurs around 80 GHz for CW
operation and 70 GHz for pulsed operation.

The performance of GaAs IMPATT diodes in CW operation has been
significantly improved recently. Efficiencies of 18 to 35 percent
have been achieved for frequencies below 44 GHz. In terms of power
output and efficiency, GaAs IMPATT diodes show better performance in
CW operation for frequencies up to 60 GHz than Si IMPATT diodes.
However, GaAs IMPATT diodes have not worked well for frequencies
higher than 100 GHz.

Because of electronic limitations, the fundamental power
available from an IMPATT diode decreases as the square of frequency
in the millimeter-wave region. Thus the available output power at
the fundamental frequency ω_1, denoted by $P_1(\omega_1)$, can be written as

$$P_1(\omega_1) = K/\omega_1^2 \ ,$$

where K is a proportionality constant. At the frequency $\omega_n = n\omega_1$
the available output power becomes

$$P_1(\omega_n) = K/\omega_n^2 = P_1(\omega_1)/n^2 \ ,$$
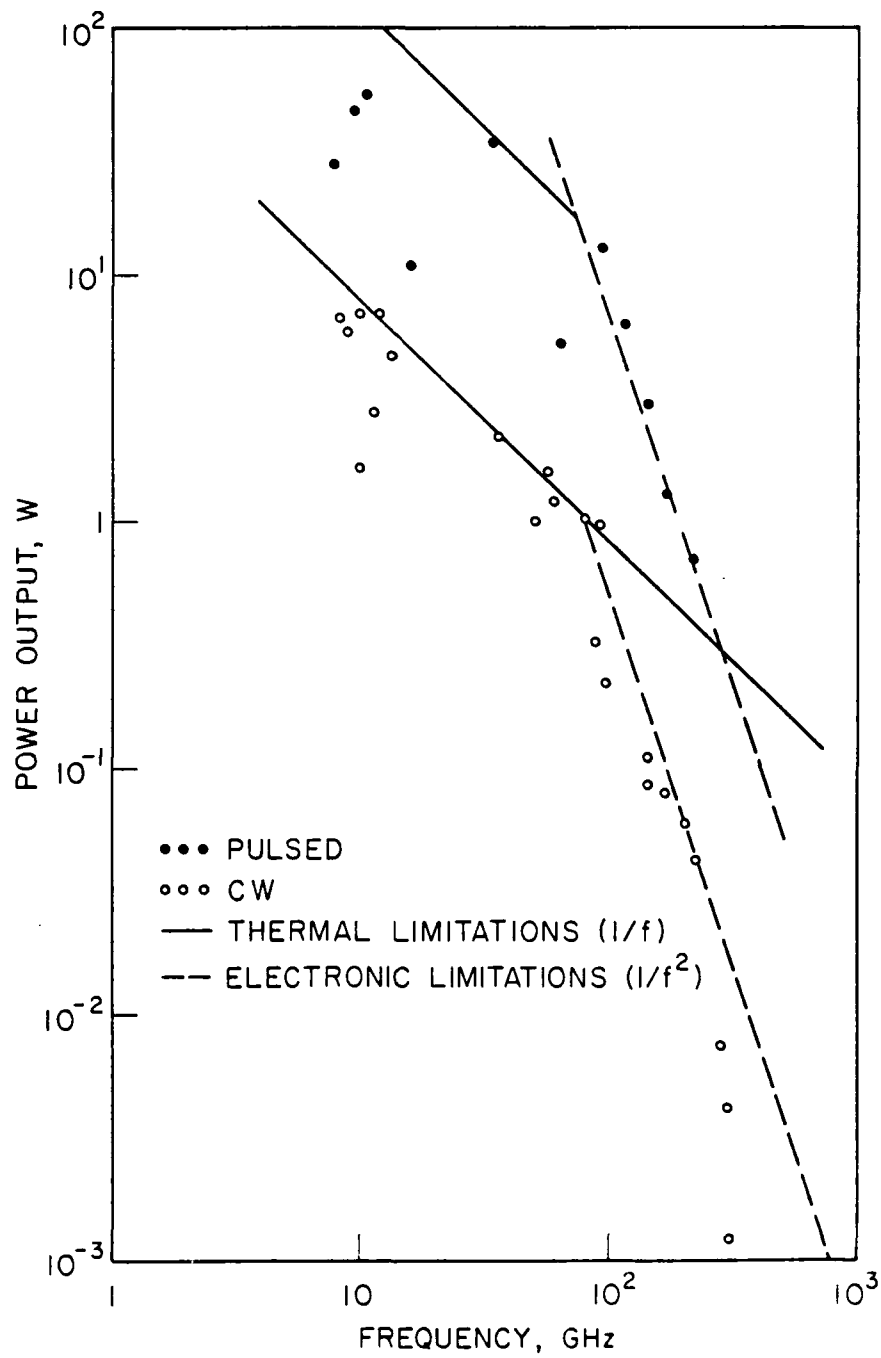
FIG. 1.1 STATE OF THE ART OF Si IMPATT DIODES.
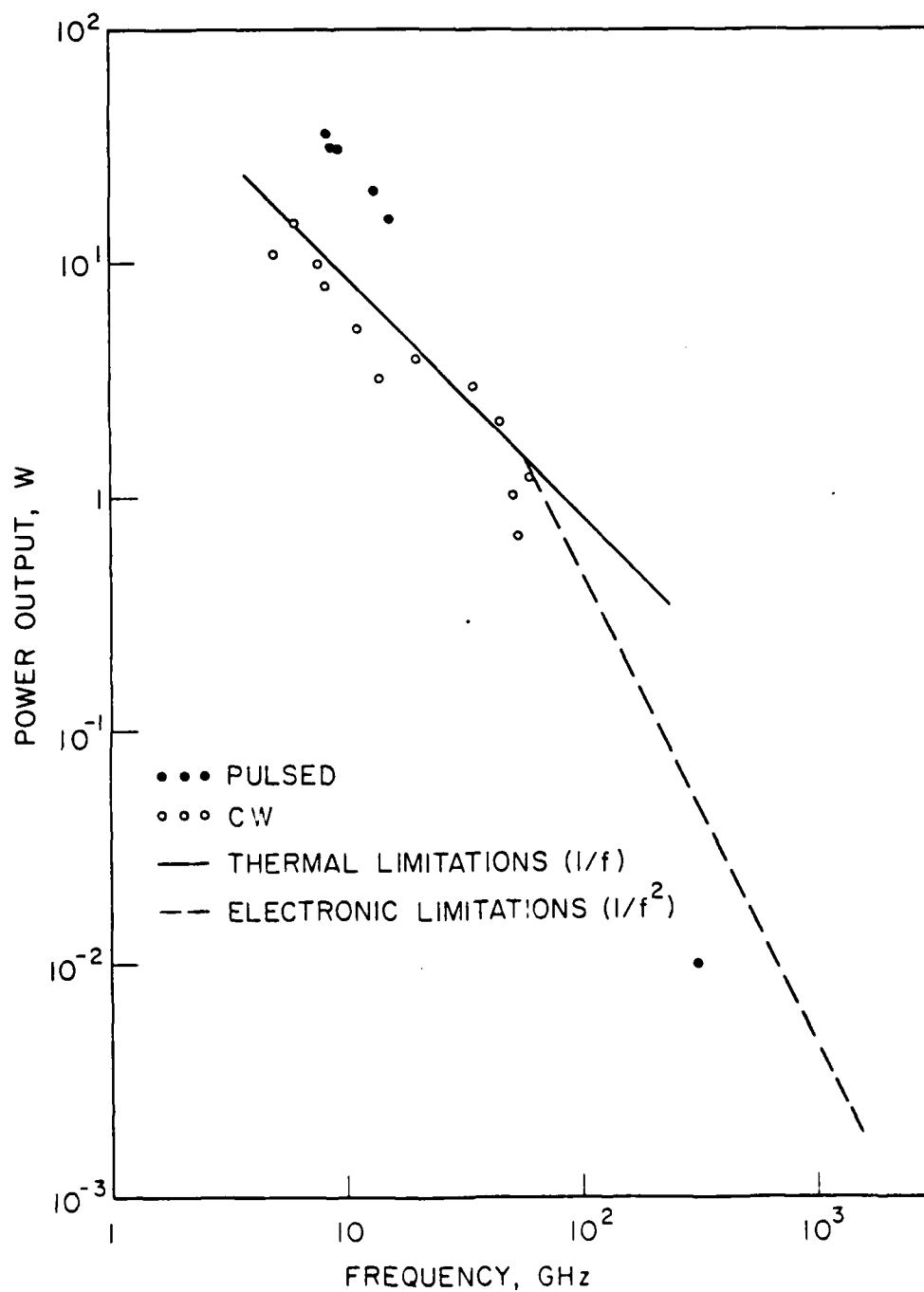
FIG. 1.2 STATE OF THE ART OF GaAs IMPATT DIODES.

where n is an integer. Since the IMPATT diode is a nonlinear
device, the output power at the frequency ω_n can also be achieved by
extracting the nth harmonic power from the IMPATT diode working at
the fundamental frequency ω_1. $P_n(\omega_n)$ is denoted as the nth harmonic
power available from the IMPATT diode self-pumped or externally
driven at the frequency ω_1. The harmonic power approach may yield
higher output power than a fundamental source if

$$P_n(\omega_n) > P_1(\omega_n)$$

is satisfied. In other words, this requires that the conversion
efficiency from the fundamental power to the desired harmonic power
$Eff_{1n}(\omega_n)$ must satisfy the following inequality:

$$Eff_{1n}(\omega_n) = \frac{P_n(\omega_n)}{P_1(\omega_1)} > \frac{1}{n^2} .$$

This inequality is the criterion for determining whether the harmonic
power approach is better than the fundamental power approach. From
the state of the art of devices, the fundamental power falls off
more quickly at very high frequencies than that expected from the
electronic limitations. Hence, the harmonic power approach may become
attractive at very high frequencies.

1.3 Simple Analysis of IMPATT Diodes

The basic large-signal characteristics of IMPATT diodes can
be understood best by considering an ideal Read diode. For an ideal
reverse-biased Read diode, its structure, electric field distribution,
and current and voltage waveforms are shown in Fig. 1.3. The
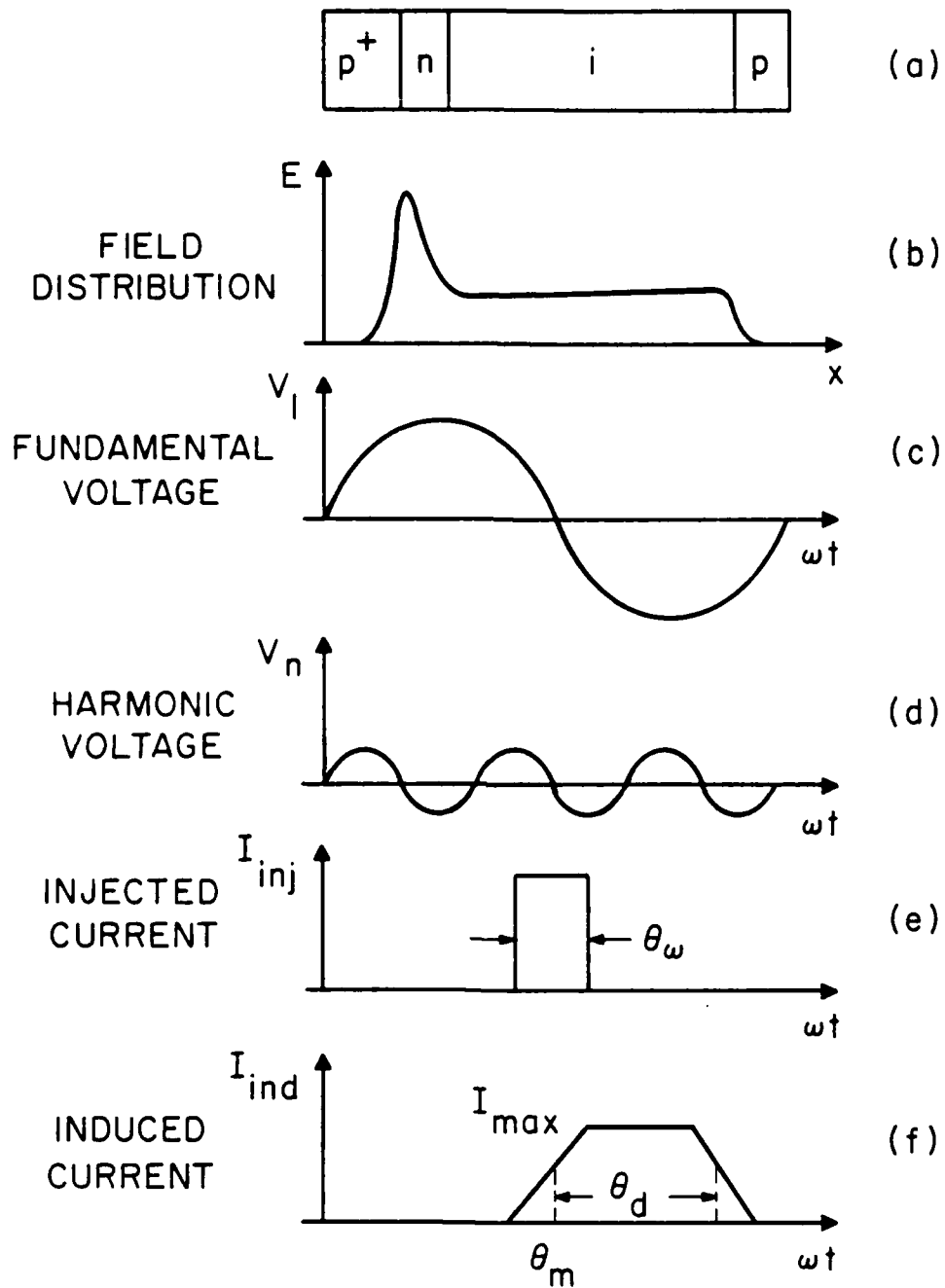
FIG. 1.3 READ DIODE STRUCTURE, FIELD DISTRIBUTION, AND
VOLTAGE AND CURRENT WAVEFORMS.

narrow n region in this Read diode is referred to as the avalanche region where the avalanche process occurs; the intrinsic region is referred to as the drift region where carriers drift at saturated velocities.

The power generation mechanism of a Read diode can be understood from Fig. 1.3. When a fundamental voltage V_1 is applied to the diode terminals, a charge carrier pulse is created in the avalanche region due to the avalanche process and is injected into the drift region. This injected pulse, peaked at $\theta_m = \pi$, moves through the drift region and is collected at the far end of the diode. The movement of the charge carriers induces a current at the device terminals. The induced current usually appears in the second half cycle of RF voltage V_1 for a properly designed diode. This implies that the induced current has a 180 degree phase angle difference relative to V_1. In other words, the diode can generate RF power.

A simple analysis for harmonic power generation of an IMPATT diode will be carried out by assuming that the imposed harmonic voltage V_n which is much smaller than the fundamental voltage (V_1) has no effect on the injected and induced current waveforms shown in Fig. 1.3. The injected current having a width of θ_ω is assumed to be symmetric about θ_m and the transit angle is given by θ_d. By taking the average of the induced current, the dc current can be obtained:

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_{ind} d\omega t = \frac{I_{max}}{2\pi} \theta_d \quad . \tag{1.1}$$

The fundamental and harmonic current phasors are

$$\tilde{I}_1 \;=\; \frac{1}{\pi}\int_0^{2\pi} I_{ind}\,e^{-j\omega t}\,d\omega t \;=\; \frac{8I_{dc}}{\theta_\omega \theta_d}\sin\left(\frac{\theta_\omega}{2}\right)\sin\left(\frac{\theta_d}{2}\right)\,e^{-j[\theta_m+(\theta_d/2)]}$$

$$(1.2)$$

and

$$\tilde{I}_n \;=\; \frac{1}{\pi}\int_0^{2\pi} I_{ind}\,e^{-j\omega t}\,d\omega t \;=\; \frac{8I_{dc}}{n^2\theta_d\theta_\omega}\sin\frac{n\theta_\omega}{2}\sin\left(\frac{n\theta_d}{2}\right)e^{-j[n\theta_m+(n\theta_d/2)]}$$

$$.\quad (1.3)$$

The dc and RF powers are

$$P_{dc} \;=\; I_{dc}V_{dc} \;=\; \frac{\theta_d I_{max}}{2\pi}V_{dc}\;, \qquad\qquad (1.4)$$

$$P_1 \;=\; -\frac{1}{2\pi}\int_0^{2\pi} V_1\sin\omega t\, I_{ind}\,d(\omega t) \;=\; -V_1 I_{dc}\,\frac{\sin(\theta_\omega/2)}{\theta_\omega/2}$$

$$\cdot\;\frac{\cos\theta_m - \cos(\theta_m+\theta_d)}{\theta_d}\quad (1.5)$$

and

$$P_n \;=\; -\frac{1}{2\pi}\int_0^{2\pi} V_n\sin(n\omega t+\phi_n) I_{ind}\,d\omega t \;=\; -V_n I_{dc}\,\frac{\sin(n\theta_\omega/2)}{n\theta_\omega/2}$$

$$\cdot\;\frac{\cos(n\theta_m+\phi_n) - \cos[n(\theta_m+\theta_d)+\phi_n]}{n\theta_d}\quad (1.6)$$

and the efficiencies are

$$Eff_1 \;=\; \frac{P_1}{P_{dc}} \;=\; -\frac{V_1}{V_{dc}}\,\frac{\sin(\theta_\omega/2)}{\theta_\omega/2}\,\frac{\cos\theta_m - \cos(\theta_m+\theta_d)}{\theta_d}$$

$$(1.7)$$

and

$$Eff_n = \frac{P_n}{P_{dc}} = - \frac{V_n}{V_{dc}} \frac{\sin(n\theta_\omega/2)}{n\theta_\omega/2}$$

$$\cdot \frac{\cos(n\theta_m + \phi_n) - \cos[n(\theta_m + \theta_d) + \phi_n]}{n\theta_d} \quad . \quad (1.8)$$

From the preceding equations several conclusions may be drawn:

1. The harmonic power, efficiency and current are inversely proportional to the harmonic number n.

2. The sharper the injected current is, the higher the harmonic power and efficiency are.

3. Higher harmonic power and efficiency can be achieved if the modulation ratio V_n/V_{dc} is high or the transit angle is small.

Based on the ideal induced-current waveform shown in Fig. 1.3, the harmonic current is usually lower than the fundamental current. However, for a practical diode, there are several mechanisms which can modify the induced current waveform and enhance the harmonic current amplitude. They are due to: (1) depletion-layer modulation, (2) asymmetric doping structure and (3) material property. For simple consideration of waveform modification, the sharp pulse approximation is adopted and the induced current has a waveform as shown in Fig. 1.4. The dc current is

$$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} I_{ind} \, d\omega t = \frac{I_{max}}{2\pi} \theta_d + \frac{A I_{max}}{2\pi} \theta_a$$

$$= \frac{I_{max}}{2\pi} (\theta_d + A\theta_a) \quad . \quad (1.9)$$

The fundamental and harmonic current phasors are
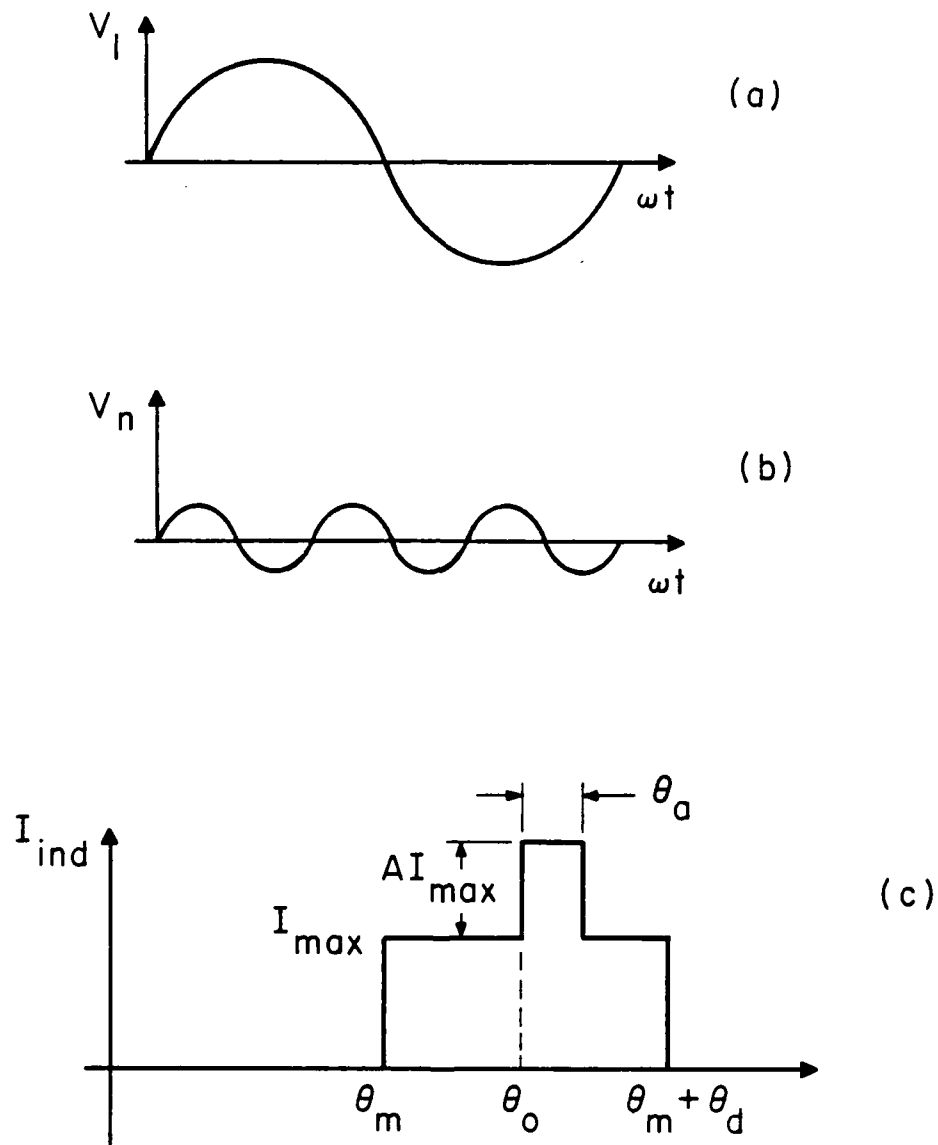
FIG. 1.4 MODIFIED INDUCED-CURRENT WAVEFORM AND VOLTAGES.

$$\tilde{I}_1 = \frac{1}{\pi} \int_0^{2\pi} I_{ind}\, e^{-j\omega t}\, d\omega t = -\frac{I_{max}}{j\pi}\left[e^{-j\theta_m}(e^{-j\theta_d} - 1)\right.$$

$$\left. + A\, e^{-j\theta_o}(e^{-j\theta_a} - 1)\right] \quad (1.10)$$

and

$$\tilde{I}_n = \frac{1}{\pi} \int_0^{2\pi} I_{ind}\, e^{-jn\omega t}\, d\omega t = -\frac{I_{max}}{jn\pi}\left[e^{-jn\theta_m}(e^{-jn\theta_d} - 1)\right.$$

$$\left. + A\, e^{-jn\theta_o}(e^{-jn\theta_a} - 1)\right] \quad . \quad (1.11)$$

The dc and RF powers are

$$P_{dc} = I_{dc}V_{dc} = \frac{V_{dc}I_{max}}{2\pi}(\theta_d + A\theta_a) \quad , \quad (1.12)$$

$$P_1 = -\frac{1}{2\pi}\int_0^{2\pi} V_1 \sin \omega t\, I_{ind}\, d\omega t = -\frac{V_1 I_{max}}{\pi}\left[\sin\left(\theta_m + \frac{\theta_d}{2}\right)\sin\frac{\theta_d}{2}\right.$$

$$\left. + A\sin\left(\theta_o + \frac{\theta_a}{2}\right)\sin\frac{\theta_a}{2}\right] \quad (1.13)$$

and

$$P_n = -\frac{1}{2\pi}\int_0^{2\pi} V_n \sin(n\omega t + \phi_n)I_{ind}\, d\omega t = -\frac{V_n I_{max}}{n\pi}$$

$$\left[\sin\left(n\theta_m + \frac{n\theta_d}{2} + \phi_n\right)\sin\frac{n\theta_d}{2} + A\sin\left(n\theta_o + \frac{n\theta_a}{2} + \phi_n\right)\sin\frac{n\theta_a}{2}\right] \quad .$$

$$(1.14)$$

The efficiencies are

$$Eff_1 = \frac{P_1}{P_{dc}} = -\frac{2V_1}{V_{dc}}\frac{1}{\theta_d + A\theta_a}\left[\sin\left(\theta_m + \frac{\theta_d}{2}\right)\sin\frac{\theta_d}{2}\right.$$

$$\left. + A\sin\left(\theta_o + \frac{\theta_a}{2}\right)\sin\frac{\theta_a}{2}\right] \quad (1.15)$$

and

$$Eff_n = \frac{P_n}{P_{dc}} = -\frac{2V_n}{nV_{dc}} \frac{1}{\theta_d + A\theta_a}\left[\sin\left(n\theta_m + \frac{n\theta_d}{2}\right)\sin\frac{n\theta_d}{2}\right.$$

$$\left. + A\sin\left(n\theta_o + \frac{n\theta_a}{2} + \phi_n\right)\sin\frac{n\theta_a}{2}\right] \quad . \quad (1.16)$$

From the preceding equations it is obvious that the harmonic power can be improved if the induced current is optimized. Furthermore, a dip in the induced current waveform ($A < 0$) can enhance significantly the harmonic power. However, the fundamental power may become negative (i.e., the device absorbs power) and the self-pumping requirement cannot be satisfied.

The preceding simple analysis reveals some factors for determining the harmonic power generation of IMPATT diodes. However, the interaction between the fundamental and harmonic signals is not negligible in an IMPATT oscillator and the device impedance level is important in the design of an IMPATT oscillator circuit. Both will be considered in detail in this study.

1.4 Outline of the Present Study

The purpose of this study is to investigate the capability of harmonic power generation from both GaAs and Si IMPATT diodes. To achieve this purpose, computer simulation and analytic equations are used to understand the behavior of IMPATT diodes in the presence of harmonic components, and waveguide circuits have been designed to measure the harmonic power from available IMPATT diodes. The measured results and theoretical calculations are compared.

A detailed outline for each chapter follows. In Chapter II, computer simulations for two-frequency operation are carried out for both GaAs and Si diodes with various doping profiles, such as uniform, hybrid, double-Read and pin structures. The simulation results for regular structures under active mode operation and pin diode structures under passive mode operation are compared in terms of the maximum dc electric field, harmonic current amplitudes, injected current width, depletion layer modulation effect, and practical design considerations (i.e., thermal and circuit matching). Guidelines of the optimum design for harmonic power generation are also given. In Chapter III, an analytic model for three-frequency operation is developed by extending Mouthaan's two-frequency model. This model with simple assumptions is used to investigate the diode behavior under multifrequency operation, the interaction between the device and the circuit, and to determine the criteria for stable oscillation and optimum loading conditions for maximum harmonic power generation. In Chapter IV, waveguide circuits for one, two and three frequencies are designed to measure the fundamental and harmonic powers for available GaAs and Si IMPATT diodes. The conversion efficiencies and harmonic powers measured are discussed in detail. In Chapter V, a summary of the investigation and suggestions for further research are given.

CHAPTER II

LARGE-SIGNAL SIMULATION OF Si AND GaAs IMPATT DIODES

2.1 Introduction

In this chapter, the nonlinear properties and related
harmonic power generation of IMPATT diodes are investigated in
detail. The nonlinear properties of the devices are characterized
by frequency-domain simulation under single-frequency and multi-
frequency operations. The device nonlinearity arises from three
main mechanisms, i.e., avalanche multiplication, the drift process,
and depletion-layer modulation. These three mechanisms, subject to
device structure and material parameters, are carefully studied and
their effects on the injected and induced current waveforms are
determined. Furthermore, the induced current is Fourier analyzed
and the effect on the harmonic content of the induced current due
to the interaction between fundamental and harmonic voltages is
examined. Harmonic power generation in these devices is emphasized.

The IMPATT device is considered for operation in two modes. In
the first mode, which is referred to as the active mode, the device
oscillates at the fundamental frequency but power is extracted from
the device at the desired harmonic. Because of the requirement of
self-oscillation, the device must be terminated at the fundamental
with a reactive load or a load having small positive resistance.
Under this situation, the harmonic power is calculated by matching
the device with 1-Ω resistance at the desired harmonic. Comparison
of harmonic power generation among various device structures, such

-23-

as double-drift Read, double-drift uniform, and double-drift hybrid

structures, is performed for Si and GaAs at the same frequency.

Each structure is punched through at breakdown and is optimized

at the same fundamental frequency. Since the device dimension is

small, heat sinking may impose a serious problem for device design.

Therefore, the thermal limitation, together with circuit-matching

considerations, will be taken into account when the harmonic power

from each structure is determined.

In the second mode of operation, a pin avalanche diode,

utilized as a frequency multiplier, is driven by an external fun-

damental source and power is extracted from it at the desired

harmonic. Since avalanche multiplication occurs uniformly through-

out the entire intrinsic region, no distinct drift region exists

in this diode. The induced current may have a sharp waveform, which

is equivalent to the case of $A > 0$ in Fig. 1.4, and the harmonic

current contained in the induced current is expected to be high,

which favors harmonic power generation. Several pin diodes with

different device lengths are investigated for their capabilities

to convert the external fundamental power to the desired harmonic

power at different dc current densities. Both circuit matching

and thermal limitations are taken into consideration when calculating

the harmonic power from each pin diode.

Throughout this simulation, the static drift-diffusion model

is employed, although it is known that for GaAs IMPATT devices,

relaxation-time effects become significant in the millimeter-wave

frequency range. The fundamental frequency chosen in this study is 23

GHz and the device temperature is assumed to be $500^{\circ}K$. The highest

harmonic considered is the third one. The phase angles of the fundamental and harmonic current and voltage phasors are measured with reference to the fundamental voltage phasor.

2.2 Description of Computer Simulation Program and Material Parameters

The computer simulation program used in this study was originally developed by Bauhahn[66] and later modified by Mains.[67] This program solves the one-dimensional transport equations including distributed avalanche multiplication of carriers and field-dependent velocities and diffusion coefficients for electrons and holes. The transport equations are as follows:

Continuity Equation for Holes

$$q \frac{\partial p}{\partial t} = G - \frac{\partial J_p}{\partial x} \ . \tag{2.1}$$

Continuity Equation for Electrons

$$q \frac{\partial n}{\partial t} = G + \frac{\partial J_n}{\partial x} \ . \tag{2.2}$$

Poisson's Equation

$$\nabla \cdot E = \frac{q}{\varepsilon} (N_D - N_A + p - n) \ , \tag{2.3}$$

where

$$J_p = q p v_p - q D_p \frac{dp}{dx} \ , \tag{2.4}$$

$$J_n = q n v_n + q D_n \frac{dn}{dx} \ , \tag{2.5}$$

$$G = \alpha_p J_p + \alpha_n J_n \ , \tag{2.6}$$

t = the time (s),

x = the distance (cm),

p = the hole density (cm^{-3}),

n = the electron density (cm^{-3}),

J_p = the hole current density (A·cm^{-2}),

J_n = the electron current density (A·cm^{-2}),

G = the impact avalanche generation rate of charge (C cm^{-3}/s),

E = the electric field intensity (V/cm),

q = the electronic charge (C),

ε = the dielectric constant (F/cm),

N_D = the donor concentration (cm^{-3}),

N_A = the acceptor concentration (cm^{-3}),

v_p = the hole velocity (cm/s),

v_n = the electron velocity (cm/s),

D_p = the diffusion coefficient of holes (cm^2/s),

D_n = the electron diffusion coefficient (cm^2/s),

α_p = the hole ionization rate (cm^{-1}), and

α_n = the electron ionization rate (cm^{-1}).

Various numerical techniques are employed to solve the transport equations to obtain dc, small-signal, and large-signal results. Upper-wind differencing is particularly used for the drift terms in the continuity equations. Dirichlet boundary conditions are employed for majority carriers at their respective inflow points; however, mixed boundary conditions are employed for minority carriers at their respective inflow points so that the sum of drift plus diffusion components of currents equals a fixed specific value (saturation current).

A diagram showing the sequence and inter-relationship among various programs[68] is illustrated in Fig. 2.1. The program MOBIN is used to generate a material parameter file needed for dc and ac simulations. The DC and AC programs are run together to obtain dc solutions. The dc solutions are either printed out or plotted by the IPLOT program. Before running the SMASIGBC program to obtain small-signal G-B data, the DCBIAS2BC program must be run to refine the dc solutions. This program employs an implicit numerical method and can obtain very accurate dc solutions. The AC and IMPEXP programs are used for large-signal ac simulations. The dc solutions serve as starting points for the ac simulation. The IMPEXP program is the only program to solve the transport equations, and an explicit numerical method is employed for this program.

Material parameters play key roles in the performance of IMPATT devices. Therefore, the parameters used for simulation should be chosen carefully so that simulation results are comparable with experimental results. However, some available experimental data for the material parameters are inconsistent, for example, the ionization rates.[69-71] These inconsistencies result in quite different simulation results.[72] Furthermore, some of the parameter values at high fields are, unfortunately, not well known. It was decided to use those adopted by Mains[73] since they result in better agreement with experimental results.

Ionization rates for electrons and holes are important parameters for IMPATT devices. The ionization rates used for Si are the data of Lee et al.[69] which show good agreement with the formulation of Baraff.[74] The ionization rates used for GaAs are

-28-
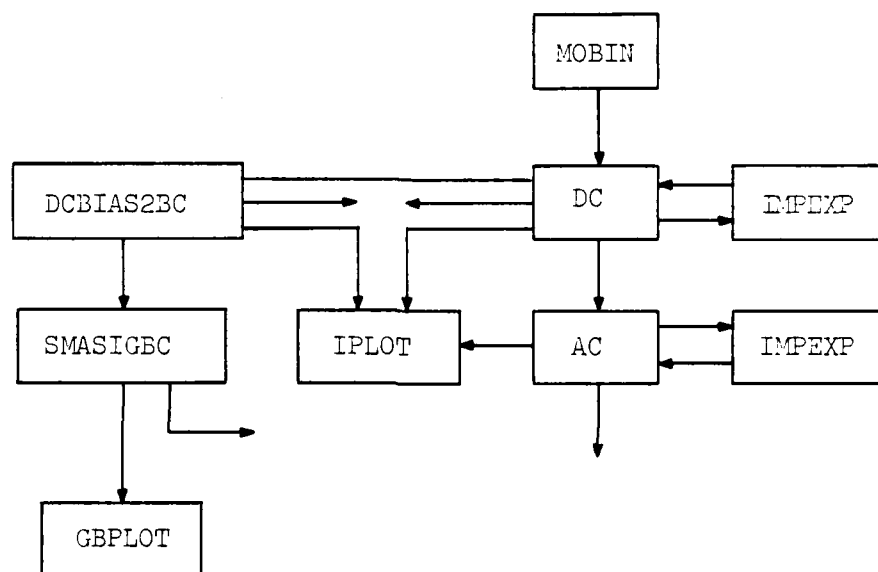
FIG. 2.1   FLOW CHART SHOWING THE SEQUENCE AND

INTERRELATIONSHIP AMONG VARIOUS PROGRAMS

USED FOR THE SIMULATION.

in accordance with the measurements carried out at Raytheon

(see Reference 73). In general, the ionization rates for electrons

and holes can be expressed as

$$\alpha_n = A_n \exp{(- b_n/E)}^m \qquad (2.7)$$

and

$$\alpha_p = A_p \exp{(- b_p/E)}^m \quad , \qquad (2.8)$$

respectively, where $m = 1$ for Si and $m = 2$ for GaAs. The drift

velocities for electrons and holes in Si have the following field-

dependent expressions:

$$v_n = v_{nsat}[1 - \exp{(- \mu_n E/v_{nsat})}] \qquad (2.9)$$

and

$$v_p = v_{psat}[1 - \exp{(- \mu_p E/v_{psat})}] \quad , \qquad (2.10)$$

and the drift velocities for electrons and holes in GaAs can be for-

mulated as

$$v_n = \frac{\mu_n|E| + v_{nsat}(E/E_v)^4}{1 + (E/E_v)^4} \qquad (2.11)$$

and

$$v_p = v_{psat}[1 - \exp{(- \mu_p/v_{psat})}] \quad , \qquad (2.12)$$

respectively. The diffusion coefficients for electrons and holes in

Si are taken to be independent of field and equal to the same

constant, i.e.,

$$D_n = D_p = k_d \, . \qquad (2.13)$$

In GaAs the electron diffusion coefficient is field-dependent

and has the following form:

$$D_n = \frac{D_{no} + D_{nsat}(E/E_d)^4}{1 + (E/E_d)^4} \; .$$

However, the hole diffusion coefficient is taken to be a constant.

The values of all parameters appearing in Eqs. 2.7 through 2.14 are listed in Table 2.1 for T = 500°K. The ionization rates as functions of electric field are plotted in Fig. 2.2 for comparison.

2.3 Active Mode Operation for Si and GaAs IMPATT Diodes

2.3.1 Introduction. Silicon and GaAs IMPATT diodes in active mode operation are investigated in detail for their capabilities of harmonic power generation. This investigation, which was carried out by computer simulation, is focused on four different diode structures: GaAs double-drift Read, GaAs double-drift uniform, Si double-drift hybrid, and Si double-drift uniform. Each structure is optimized at the frequency of 23 GHz in single-frequency operation. The optimized dc current density and doping profile are used in subsequent simulations for the calculation of harmonic power for each structure. There are several reasons for using these optimized quantities: (1) It is believed that, for a given doping profile, an IMPATT diode will achieve uniquely a maximum efficiency at the corresponding optimum frequency and dc current density in single-frequency operation. Therefore, the optimum condition becomes the only reference point for comparison of device harmonic performance; other conditions make the comparison complicated. (2) The increase of dc current density imposes a

Table 2.1

Material Parameters for Si and GaAs at T = 500°K

	μ_n (cm²/V-s)	μ_p (cm²/V-s)	v_{nsat} (cm/s)	v_{psat} (cm/s)	E_v (V/cm)
Si	550	250	8.5×10^6	1.02×10^7	--
GaAs	4000	200	5×10^6	5.2×10^6	4×10^3

	D_{no} (cm²/s)	D_{nsat} (cm²/s)	D_n (cm²/s)	D_p (cm²/s)	E_d (V/cm)
Si	--	--	18.2	18.2	--
GaAs	172	15	--	15	5.8×10^3

	A_n (cm⁻¹)	b_n (V/cm)	A_p (cm⁻¹)	b_p (V/cm)
Si	1.8×10^6	1.64×10^6	1×10^7	5.2×10^6
GaAs	1.84×10^5	6.47×10^5	1.84×10^5	6.47×10^5

-32-
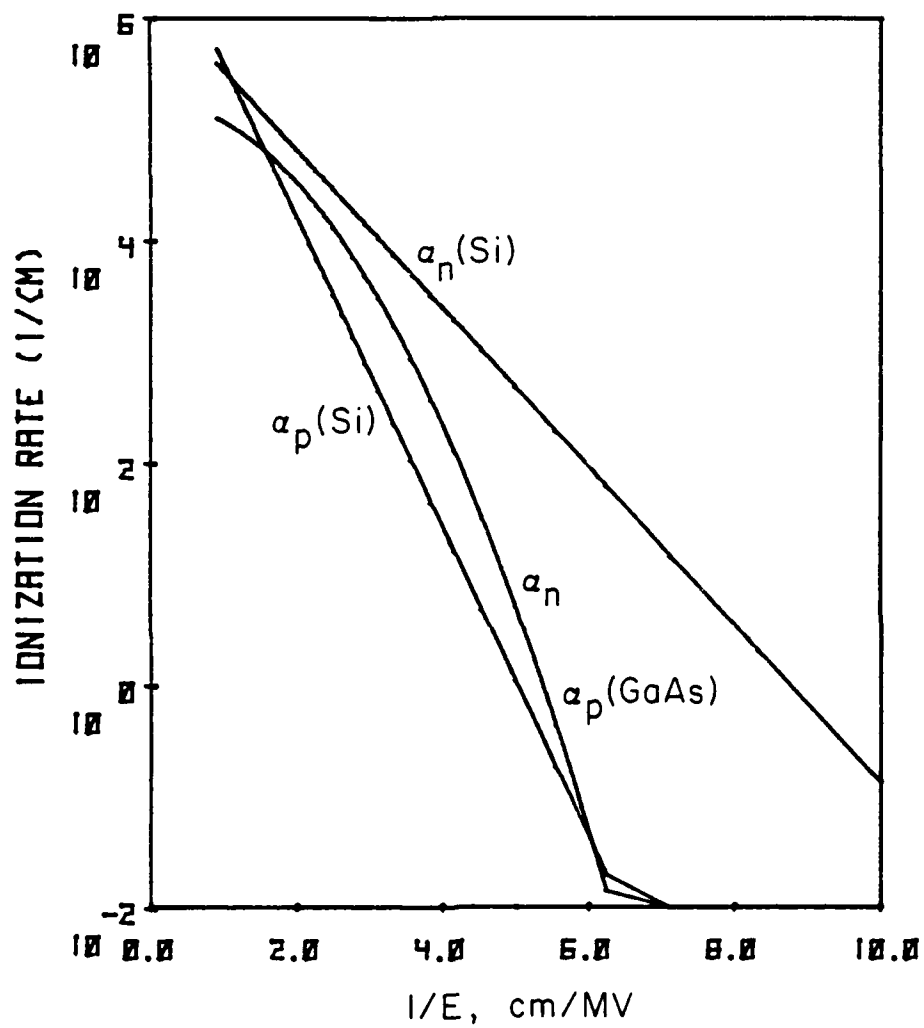
FIG. 2.2 IONIZATION RATES VS. THE RECIPROCAL OF

ELECTRIC FIELD.

serious thermal problem on device operation due to the temperature
rise and degrades the fundamental efficiency due to space-charge
effects. Therefore, it is best to operate the diode at its optimum
dc current density. (3) It may not be practical to operate the
diode at a frequency lower than the optimum one, even though the
harmonic power generation from the device may be improved if the
operating fundamental frequency is low.

The nonlinearity of diodes in single-frequency operation is
studied first. Since the diodes are only driven by a fundamental
voltage, there is no interaction due to the harmonic voltage.
Therefore, the study for single-frequency operation is mainly con-
cerned with the fundamental and harmonic currents contained in the
induced current. All the factors, such as depletion-layer modula-
tion, drift process, and avalanche multiplication, that affect
harmonic current generation are examined. Comparison of harmonic
current generation among all the diodes at various fundamental
voltages is made in terms of the effects of avalanche multiplica-
tion on the injected current waveform and the drift and depletion-
layer modulation on the induced current waveform. These effects
are dependent on the doping profile. Hence, it is necessary to
determine the role of the doping profile on the device performance.
Conclusions from this study will be useful in discussing multi-
frequency operation.

While carrying out multifrequency simulation, only the
fundamental voltage and one harmonic voltage (the third-harmonic
voltage in most cases) are included for simulation. The resulting
voltage waveform is different from the sinusoidal one. The

nonsinusoidal voltage waveform gives rise to significant effects on the injected and induced current waveforms, particularly when the fundamental voltage is high. More precisely, the interaction between two voltages affects the harmonic current generation of diodes. A detailed explanation about this interaction is given in accordance with the observations from single-frequency operation. Comparison of the maximum attainable harmonic power among diodes is carried out in terms of this interaction. Furthermore, circuit-matching and thermal limitations are considered when evaluating the harmonic power from each diode. A guideline of device design for achieving the optimum harmonic power output is given.

2.3.2 Diode Structure for Operation at 23 GHz. Four different diodes have been designed to operate at the fundamental frequency of 23 GHz. The major factors involved in diode design are the saturated velocities and loss in an undepleted region.

For GaAs and Si diodes, the loss in the undepleted region is more severe in the p-side than in the n-side because of the lower mobilities of holes. Therefore, the p-side is usually kept punched through to minimize the loss in the undepleted region of this side caused by a high RF voltage. The electric field intensity at the p-side contact is maintained around 0.25 E_c at breakdown, where E_c is the critical electric field intensity at the metallurgical junction. For the n-side, the optimum punch-through factor is not easily determined since the depletion-layer modulation may enhance the performance of GaAs diodes.[75] For further consideration of harmonic operation, the device impedance at the desired harmonic frequency is small, so any loss in the undepleted region will

deteriorate harmonic output power. Hence, in the preliminary design, each diode is punched through at breakdown and the electric field intensities at the contacts are kept around $0.25 \ E_c$.

When choosing a device length for each diode, the shift of the avalanche region center away from the metallurgical junction due to the unequal ionization rates and asymmetric doping profile[76] should be taken into account. The spread of the avalanche region is another factor to be considered. For GaAs Read and Si hybrid diodes, the avalanche region is narrow due to their specific doping profiles, and avalanche multiplication is localized. Carriers generated in a narrow avalanche region can have a uniform transit time. Therefore, the drift region transit angle θ_d is chosen to be

$$\theta_d = 2\pi f \tau_d = 0.7\pi \quad ,$$

where θ_d is the transit time of the carriers and f is the fundamental frequency. The reason for choosing this value of θ_d instead of the optimum transit angle 0.74π is to completely collect the moving particles before the next RF cycle begins and to enhance the harmonic current generation expected by Eq. 1.3.

For GaAs and Si uniform diodes, the avalanche region is much wider and the carriers generated from this wide avalanche region have a spread of transit times. It is found that if $\theta_d = 0.5\pi$ to 0.6π, each diode can be optimized at the desired frequency. The drift region length ℓ_d can be evaluated from the following formula:

$$\theta_d = 2\pi f \frac{\ell_d}{v_s} \quad , \tag{2.15}$$

where v_s is the saturated drift velocity of a carrier. The procedure to determine the optimum condition for the diodes is as follows:

1. For a given dc current density, the doping concentration is adjusted such that the electric field intensities at the contacts are close to $0.25\ E_c$.

2. For a fixed frequency (say 23 GHz), the RF voltage is varied until the efficiency reaches a maximum value.

3. When the RF voltage is the same as that in step 2, the dc current density is changed to determine the optimum value.

4. When the information obtained from steps 2 and 3 is used, the frequency is adjusted to determine the optimum.

5. If the optimum frequency is not the one desired, the device length is changed and the preceding steps are repeated until the optimum frequency is the desired one.

The optimum device structures are shown in Fig. 2.3 and some information on the diodes obtained from dc simulation at their respective optimum conditions is listed in Table 2.2. Actually, the GaAs Read diode is only optimized at 22 GHz, since this diode has a similar structure to the GaAs diode used for the measurement. It is seen from the table that the GaAs uniform diode has the highest optimum dc current density. This can be understood by the fact that the GaAs uniform diode has a high doping concentration which reduces the space-charge effect and GaAs has a small $d\alpha/dE$.

2.3.3 Comparison of the Diode Characteristics in Single-Frequency Operation. The device properties, in general, are dependent on physical parameters, such as doping profile, device temperature, and material parameters, and terminal electric conditions, such as
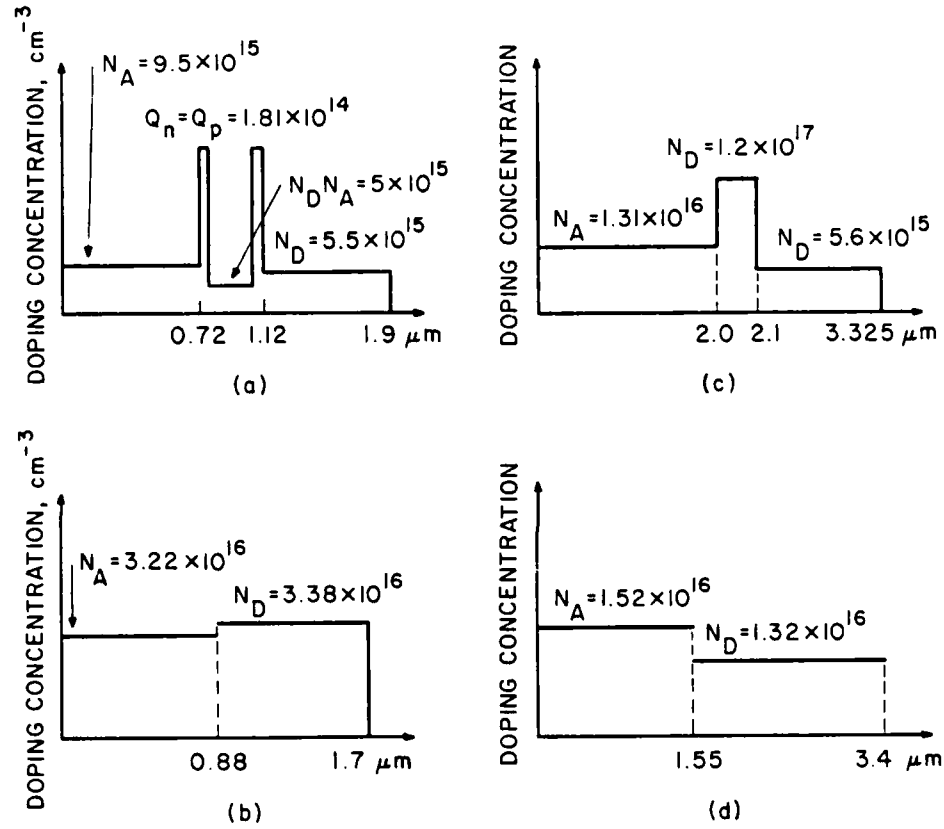
FIG. 2.3 DIODE STRUCTURES USED FOR SIMULATION.

(a) GaAs DOUBLE-DRIFT READ STRUCTURE,

(b) GaAs DOUBLE-DRIFT UNIFORM STRUCTURE,

(c) Si DOUBLE-DRIFT HYBRID STRUCTURE AND

(d) Si DOUBLE-DRIFT UNIFORM STRUCTURE.

Table 2.2

Dc Parameters for the Diodes Investigated

(E_L = the electric field at the p-side contact; E_R = the electric field at the n-side contact;

E_c = the electric field at the junction; x_a = the avalanche region width; x_n, x_p = the drift

region width for electrons and holes, respectively; and

θ_{dn}, θ_{dp} = the drift angles for electrons and holes, respectively)

Diode	E_c (10^5 V/cm)	E_L (10^5 V/cm)	E_R (10^5 V/cm)	x_n (μm)	x_p (μm)	x_a (μm)	θ_{dn}	θ_{dp}	J_{dc} (A/cm²)	V_{dc} (V)
Si double-drift hybrid	4.67	1.0	1.158	1.275	1.5	0.45	0.69π	0.68π	1600	78.7
Si double-drift uniform	4.26	1.03	0.94	1.025	1.35	1.025	0.56π	0.6π	2400	86.06
GaAs double-drift Read	5.1	1.56	1.52	0.82	0.80	0.24	0.75π	0.74π	1256	44.76
GaAs double-drift uniform	4.75	1.25	1.26	0.56	0.58	0.56	0.52π	0.53π	3200	49.26

dc biased current density, terminal RF voltage, and frequency. The device property can be only a function of the RF terminal voltage if other conditions are fixed. The RF voltage in a practical IMPATT diode oscillator usually contains not only the fundamental voltage but also the harmonic voltages. However, the harmonic voltages are assumed to be zero while carrying out computer simulations for single-frequency operation. Thus, the fundamental voltage is the only voltage across the diode terminal, except the dc voltage. This situation is equivalent to the case where all the harmonics are short circuited and thus no harmonic power is generated. Since the driving RF voltage is well defined, the simulation results can offer a significant amount of information to understand device nonlinearity.

Simulation results are presented and discussed in the following order: (1) the fundamental device properties, including the fundamental current generation, RF power, efficiency, admittance and impedance; (2) the harmonic current; and (3) the possible mechanisms affecting the fundamental and harmonic currents. While dealing with RF current, the displacement current is neglected because it makes no contribution to RF power generation.

2.3.3a Fundamental Properties of Diodes. Listed in Tables 2.3 and 2.4 are dc voltage V_{dc}, dc current density J_{dc}, efficiency Eff_1, fundamental current density J_1, and phase angle of the fundamental current phasor relative to the fundamental voltage phasor denoted as θ_{1I} for each diode. These quantities are plotted in Figs. 2.4 to 2.9 against the normalized fundamental voltage V_{1N} (same as voltage modulation ratio) defined as

Table 2.3

Large-Signal Solutions for GaAs Read and Uniform Diodes in Single-Frequency Operation

(a) GaAs Read Diode

V_1 (V)	V_{dc} (V)	J_{dc} (A/cm²)	Eff (%)	P_1 (W/cm²)	J_1 (A/cm²)	θ_{1I} (Deg.)	J_2 (A/cm²)	θ_{2I} (Deg.)	J_3 (A/cm²)	θ_{3I} (Deg.)
1.0	44.8	1195	0.07	0.0	88	-150.1	2	137.0	1	158.1
12.0	44.7	1267	7.85	4.4	888	-146.6	80	15.2	14	-119.4
28.0	44.0	1232	27.41	14.9	1254	-147.9	194	32.5	109	-138.2
31.0	43.3	1244	29.66	16.0	1206	-148.7	233	64.9	230	-137.8
32.0	42.3	1248	23.86	12.6	858	-156.5	658	107.8	678	-141.9
32.2	41.2	1227	15.49	7.8	487	-176.4	1120	114.5	1038	-142.7
32.4	39.9	1215	4.33	2.1	234	123.5	1535	109.8	1206	-153.7
32.6	38.9	1220	-4.94	-2.3	380	67.8	1795	106.6	1268	-159.4
33.0	37.4	1213	-20.19	-9.2	781	44.6	2146	103.0	1322	-167.0

(b) GaAs Uniform Diode

V_1 (V)	V_{dc} (V)	J_{dc} (A/cm²)	Eff (%)	P_1 (W/cm²)	J_1 (A/cm²)	θ_{1I} (Deg.)	J_2 (A/cm²)	θ_{2I} (Deg.)	J_3 (A/cm²)	θ_{3I} (Deg.)
1.0	49.3	3225	0.07	0.1	336	-129.1	7	141.3	6	176.0
10.0	49.3	3137	5.07	7.8	2492	-129.0	333	43.7	54	-99.6
20.0	48.8	3143	14.57	22.4	3398	-131.1	714	42.6	209	-107.8
30.0	45.8	3112	21.26	30.3	3077	-131.0	1187	92.5	961	-125.0
32.0	45.3	3206	21.48	31.0	2885	-132.2	1594	105.9	1374	-125.9
34.0	44.2	3194	20.50	28.9	2367	-135.9	2239	117.5	1935	-126.3
37.0	42.1	3106	12.27	16.0	884	-168.9	4183	129.2	3320	-127.2
37.6	41.3	3133	7.35	9.5	611	145.8	4954	130.2	3797	-127.9
38.0	40.0	3117	-1.24	-1.5	1095	85.7	5986	131.1	4374	-128.9

Table 2.4

Large-Signal Solutions for Si Hybrid and Uniform Diodes in Single-Frequency Operation

(a) Si Hybrid Diode

V_1 (V)	V_{dc} (V)	J_{dc} (A/cm^2)	Eff (%)	P_1 (W/cm^2)	J_1 (A/cm^2)	θ_{1I} (Deg.)	J_2 (A/cm^2)	θ_{2I} (Deg.)	J_3 (A/cm^2)	θ_{3I} (Deg.)
1.0	78.6	1599	0.04	0.1	146	-135.6	1	26.6	0	-135.3
15.0	77.9	1612	6.99	8.8	1553	-138.9	185	19.8	46	-82.7
25.0	76.9	1562	14.63	17.6	1801	-141.4	287	17.4	106	-97.4
35.0	75.5	1560	22.10	26.0	1866	-142.8	338	28.8	190	-118.8
42.0	74.1	1599	25.99	30.8	1795	-144.8	437	63.0	377	-141.6
48.0	72.1	1601	24.42	28.2	1333	-151.8	986	96.0	809	-154.4
50.0	68.8	1597	15.67	17.2	724	-162.1	1684	102.8	1135	-158.7
51.0	65.6	1592	4.43	4.6	235	140.5	2272	103.9	1314	-162.3
52.0	63.1	1585	-7.69	-7.7	576	59.1	2736	103.5	1394	-166.1

(b) Si Uniform Diode

V_1 (V)	V_{dc} (V)	J_{dc} (A/cm^2)	Eff (%)	P_1 (W/cm^2)	J_1 (A/cm^2)	θ_{1I} (Deg.)	J_2 (A/cm^2)	θ_{2I} (Deg.)	J_3 (A/cm^2)	θ_{3I} (Deg.)
1.0	86.5	2407	0.02	0.0	147	-119.0	19	-0.2	12	-4.7
15.0	85.8	2333	5.22	10.4	1990	-134.4	223	38.5	48	-51.0
30.0	84.1	2321	14.92	29.1	2612	-138.0	446	34.7	173	-96.2
40.0	82.4	2344	21.44	41.4	2711	-139.8	533	45.3	297	-115.2
51.0	79.6	2429	26.66	51.6	2516	-143.5	873	85.6	733	-139.4
54.0	78.5	2315	26.80	48.7	2139	-147.5	1151	99.6	974	-143.8
62.0	74.8	2330	19.70	34.3	1111	-175.7	2678	112.5	1871	-152.3
65.0	70.2	2435	2.53	4.3	863	98.8	4262	112.3	2515	-157.1
65.4	68.7	2438	-4.68	-7.8	1191	78.4	4691	111.7	2639	-158.5
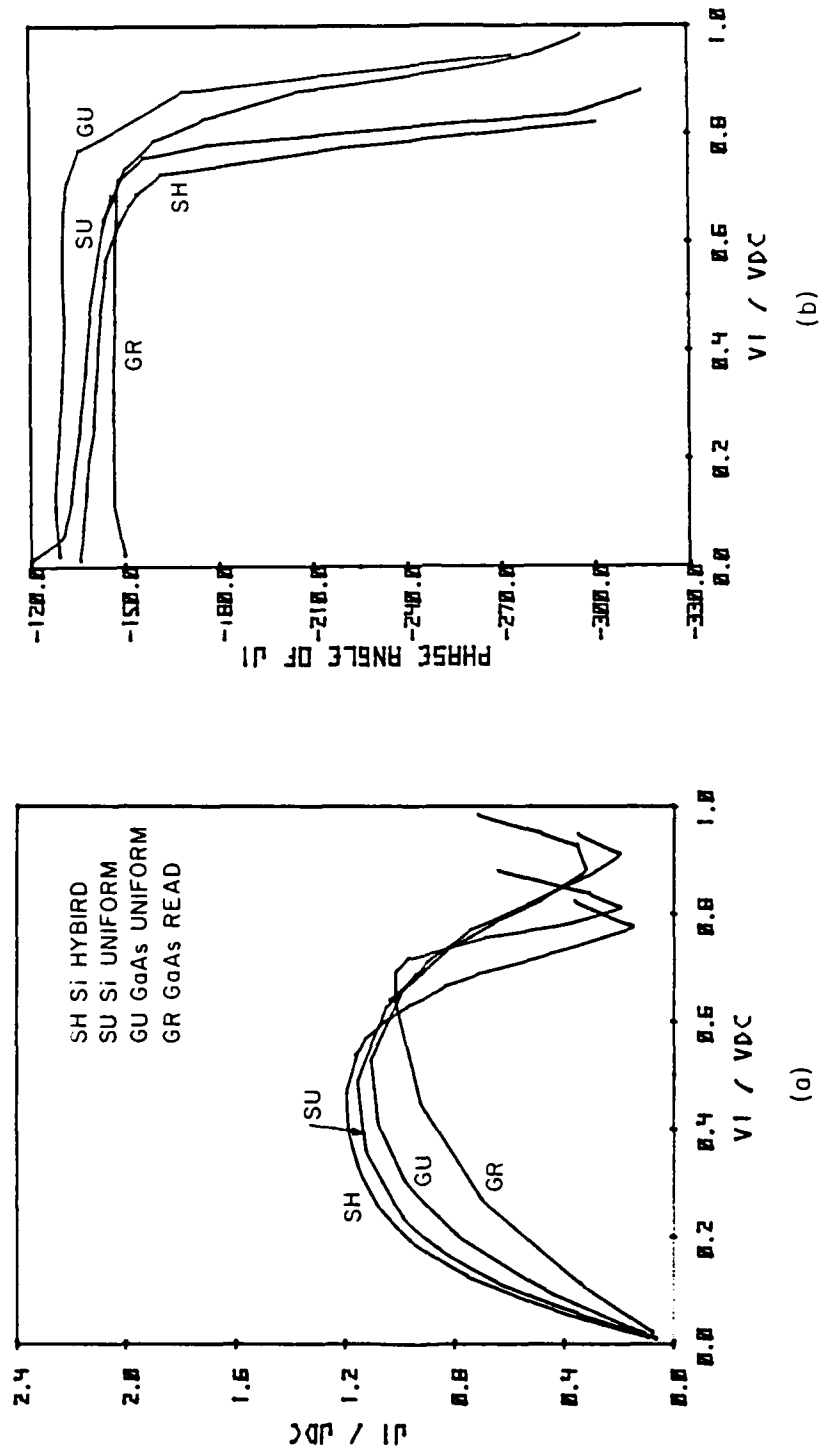
FIG. 2.4   (a) NORMALIZED FUNDAMENTAL CURRENT VS. NORMALIZED FUNDAMENTAL VOLTAGE AND (b) FUNDAMENTAL

CURRENT PHASE ANGLE VS. NORMALIZED FUNDAMENTAL VOLTAGE.
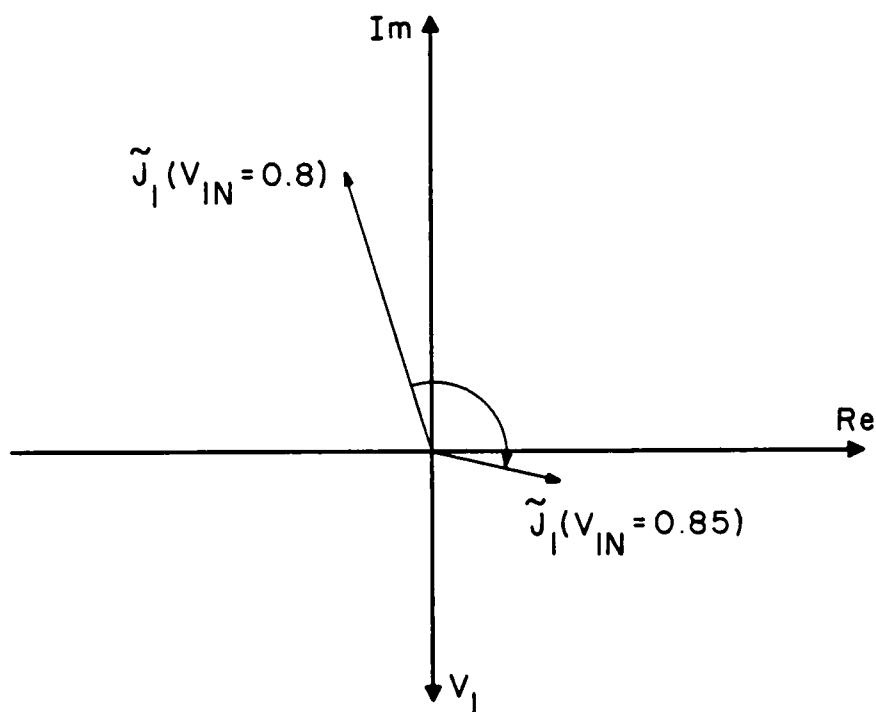
FIG. 2.5 A PHASOR DIAGRAM FOR THE FUNDAMENTAL CURRENT OF

THE GaAs READ DIODE AT V_{1N} = 0.8 AND 0.85 V.
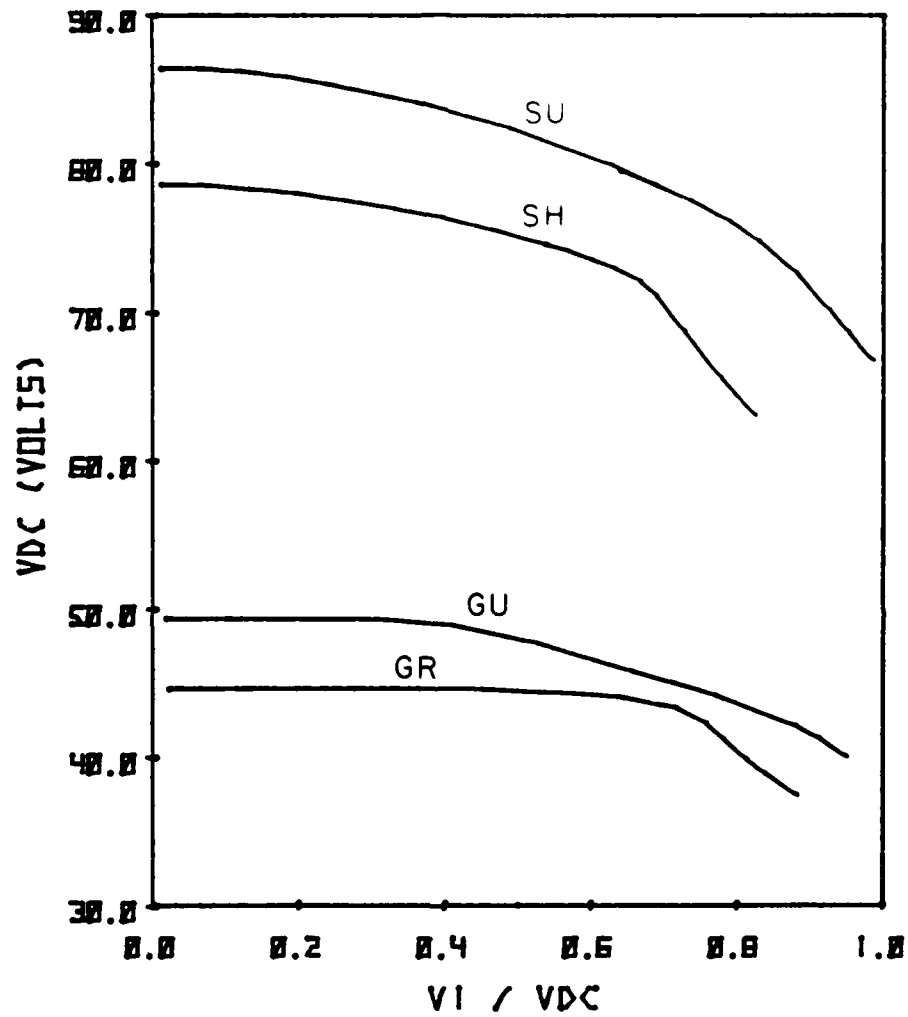
FIG. 2.6 Dc VOLTAGE VS. NORMALIZED FUNDAMENTAL VOLTAGE.
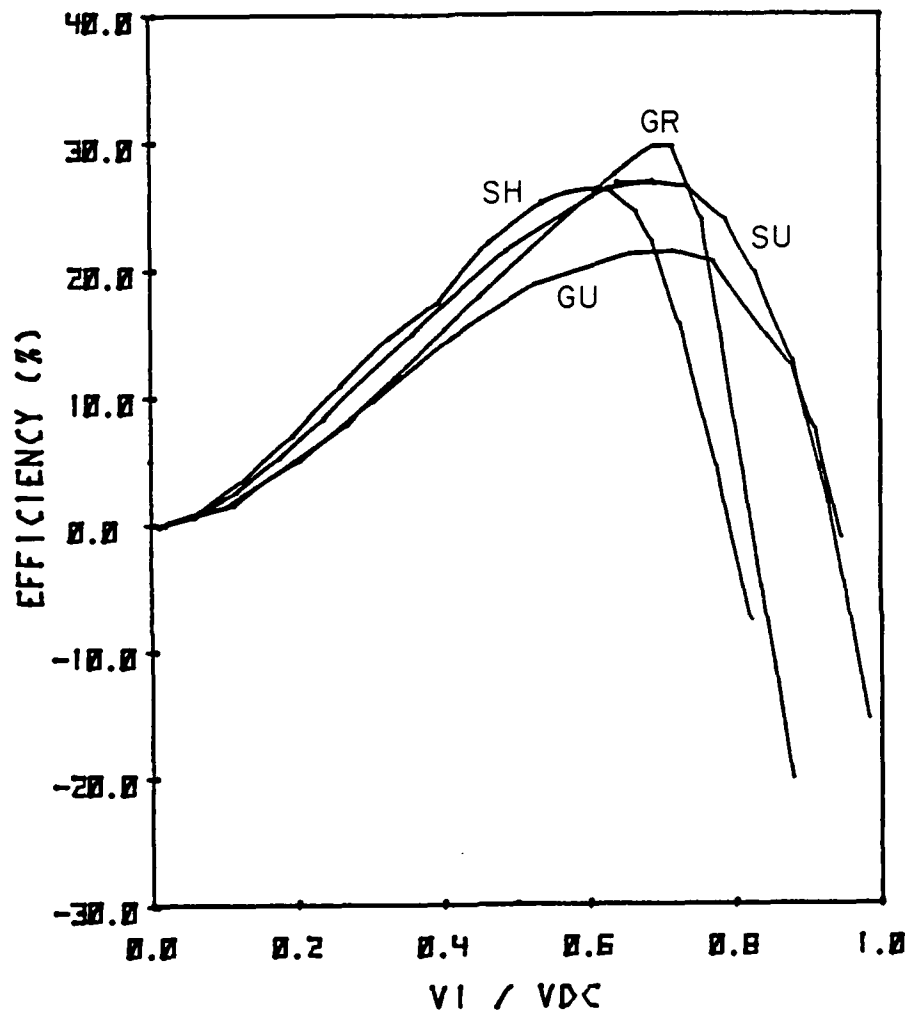
FIG. 2.7 FUNDAMENTAL EFFICIENCY VS. NORMALIZED FUNDAMENTAL
VOLTAGE.
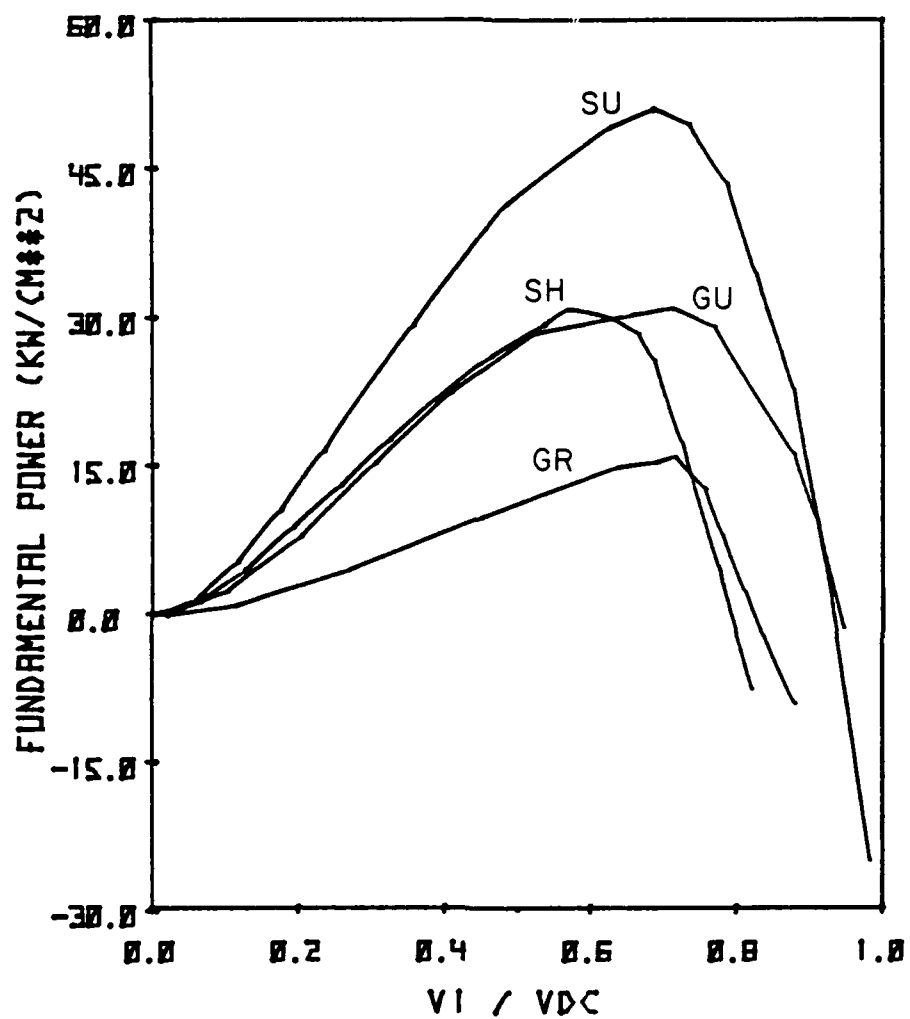
FIG. 2.8 FUNDAMENTAL POWER DENSITY VS. NORMALIZED FUNDAMENTAL

VOLTAGE.
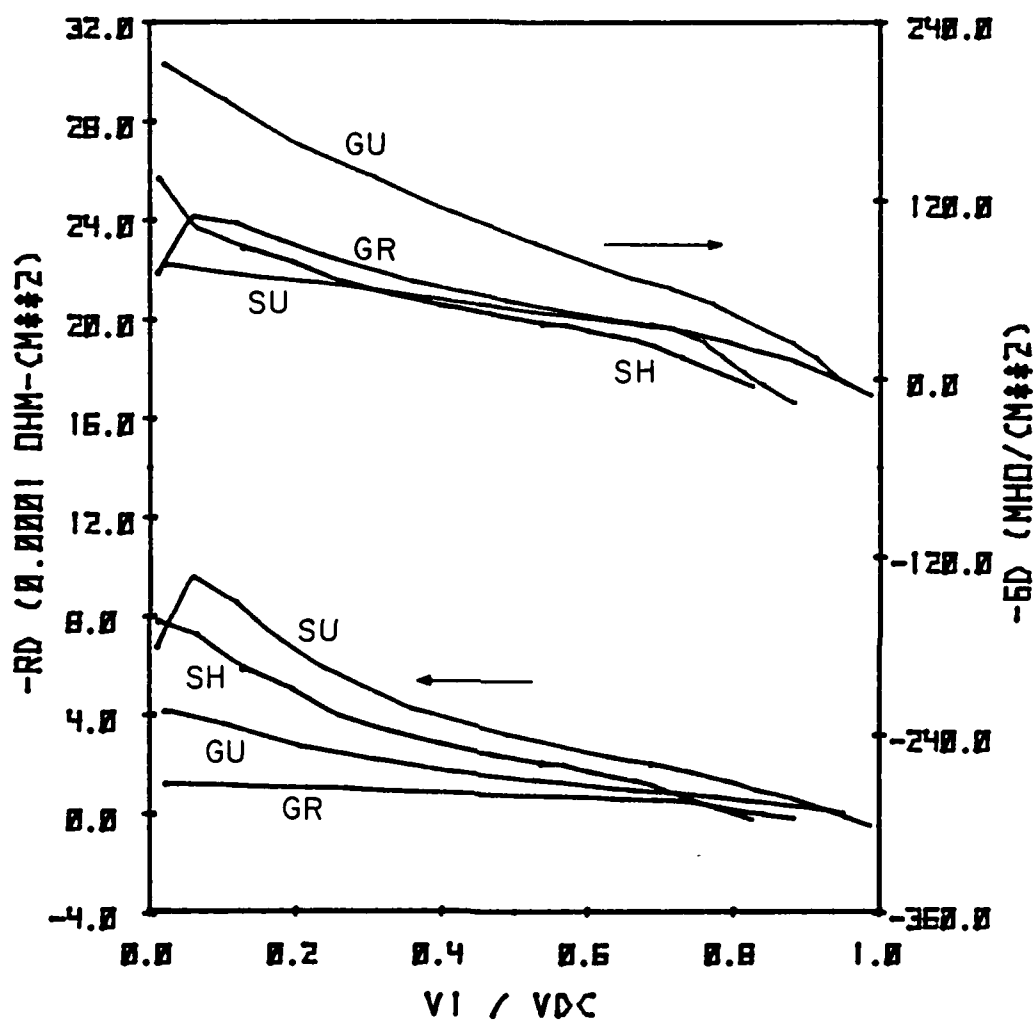
FIG. 2.9 NEGATIVE DEVICE RESISTANCE AND CONDUCTANCE VS. V_{1N}.

$V_{1N} = V_1/V_{dc}$. V_{1N} is roughly proportional the ratio of the maximum electric field swing to the average dc electric field, and it is more convenient to compare the fundamental properties of diodes in terms of V_{1N} rather than V_1. Similarly, the normalized fundamental current J_{1N}, defined as $J_{1N} = J_1/J_{dc}$, is more meaningful for comparison than J_1. It is possible to express all quantities of interest in terms of V_{1N} and J_{1N}. The deivce conductance G_{d1} is defined as

$$G_{d1} = \frac{J_1 \cos \theta_{1I}}{V_1} \; ; \tag{2.16}$$

consequently,

$$G_{d1} = \frac{V_{dc}}{J_{dc}} \frac{J_{1N}}{V_{1N}} \cos \theta_{1I} \; . \tag{2.17}$$

The efficiency can be expressed as

$$Eff_1 = -\frac{V_1 J_1 \cos (\theta_{1I})}{2V_{dc} J_{dc}} = -\frac{1}{2} V_{1N} J_{1N} \cos (\theta_{1I}) \tag{2.18}$$

and the RF power is

$$P_1 = -\frac{1}{2} G_{d1} V_1^2 = -\frac{1}{2} G_{d1} V_{1N}^2 V_{dc}^2 \tag{2.19}$$

or

$$P_1 = Eff_1 V_1 J_{dc} \; . \tag{2.20}$$

From these formulas, it is clear that the normalized fundamental current plays an essential role in device fundamental performance. This is discussed in detail next.

1. Fundamental Current. Figures 2.4a and 2.4b show J_{1N} and θ_1 as functions of V_{1N}, respectively. The curves of J_{1N} are similar to one another. Each J_{1N} exhibits a linear dependence on V_{1N} for

small V_{1N}. Obviously, this is the consequence of small perturbation. As V_{1N} increases, J_{1N} increases and then saturates when V_{1N} is between 0.4 and 0.7. J_{1N} changes little over a wide range of V_{1N}, but starts to decrease as V_{1N} exceeds the optimum voltage modulation ratio V_{1NP}, where the efficiency is maximum. The decreasing rate of J_{1N} is different for each diode. The GaAs Read diode has the highest decreasing rate, but the GaAs and Si uniform diodes show a slow decrease in J_{1N}. As V_{1N} exceeds a certain value, J_{1N} increases again, but the corresponding efficiency becomes negative. Generally speaking, except for minor differences among the diodes, all the J_{1N} curves have a similar shape over the range of V_{1N} = 0 to V_{1N} = 1. The flatness of the J_{1N} curves could be expected by the sharp-pulse model, but the fall off in the curves could not be predicted by this model. It means that there is an additional mechanism, not included in this model, responsible for the fall off. The additional mechanism is due to the depletion layer which will be discussed later.

It is seen from Fig. 2.4a that each J_{1N} has a maximum value between 1.0 and 1.2. Before the decrease of J_{1N} the Si hybrid diode has a higher J_{1N} than other diodes and the GaAs Read diode has the lowest J_{1N}. The existing maximum limit in the magnitude of J_{1N} partly results from the fact that the induced current J_{ind} at the maximum fundamental current point is positive over the whole RF cycle. According to the definition, J_1 is expressed as

$$J_1 = \left| \frac{1}{\pi} \int_0^{2\pi} J_{ind} e^{-j\omega t} \, d\omega t \right| . \qquad (2.21)$$

Since the induced current is positive, the following inequality
holds:

$$J_1 \;\leq\; \frac{1}{\pi} \int_0^{2\pi} |J_{ind}| \, d\omega t \;\leq\; \frac{1}{\pi} \int_0^{2\pi} J_{ind} \, d\omega t \;=\; 2J_{dc} \;.$$

<div align="right">(2.22)</div>

Dividing both sides of Eq. 2.22 with J_{dc} yields

$$J_{1N} \;\leq\; 2 \;.$$

<div align="right">(2.23)</div>

Although this inequality may not be valid for the case in which the
induced current becomes negative for a part of the RF cycle, it is
unfortunately true for most operating conditions in conventional IMPATT
diodes. The equal sign in Eq. 2.23 can be held only if the induced
current is an impulse, which is impossible to achieve for a diode
having a finite transit time. Usually J_{1N} is much smaller than two.
This places a limitation on fundamental power generation in a conven-
tional IMPATT diode.

The phase angle of the fundamental current phasor θ_{1I} provides
other information on device behavior. Figure 2.4b shows plots of θ_{1I}
vs. V_{1N}. It is seen that θ_{1I} for the GaAs diodes is almost flat over
a wide range of V_{1N}. However, a slight change in θ_{1I} for Si diodes
is observed. Each θ_{1I} shows a significant fall off as V_{1N} exceeds a
certain level. Consequently, the phase between the current and the
voltage eventually will be larger than 270 degrees and the efficiency
will become negative. Before the fall off occurs, there is a differ-
ence in the magnitude of θ_{1I} among the diodes which is partly due to
the difference in transit times. A phasor diagram showing the funda-
mental components of the induced current for the GaAs Read diode at

various values of V_{1N} is shown in Fig. 2.5. Since all the diodes
exhibit a similar relationship between the fundmental current phasor
and the fundamental voltage, this figure is sufficient to display how
the fundamental current phasor varies with V_{1N}. It can be seen from
the figure that the current phasor stays in the second quadrant with
little shift for V_{1N} less than 0.8 and rotates clockwise to the fourth
quadrant as V_{1N} increases.

2. Dc voltage. Figure 2.6 shows the dc voltage vs. V_{1N} for the
diodes investigated. Each V_{dc} curve declines gradually as V_{1N} increases.
This phenomenon is referred to as the back-bias effect, which is the
consequence of the highly nonlinear ionization rates in diodes. V_{dc}
must be decreased in order that the amount of charge generated in the
positive half cycle of RF voltage due to avalanche multiplication is
equal to the amount of charge removed during the other half cycle.
This effect is, of course, dependent on the ionization rates, their
first and second derivatives with respect to field, and doping profile.
A first-order expression for back-bias voltage[77] is given by

$$V_{bb} = - \frac{\alpha''}{\alpha'} (V_1/w)^2 \quad , \tag{2.24}$$

where V_{bb} is the back-bias voltage, w is the depletion-layer width,
and α' and α'' are the first and second derivatives of the ionization
rates, respectively. As shown in Fig. 2.6, the GaAs Read diode has
a very small V_{bb} for $V_{1N} < V_{1NP}$, which is related to its small α''.
In other words, the ionization rates are not as nonlinear as in Si.
The rapid fall off of V_{dc} for $V_{1N} > V_{1NP}$ is explained later.

3. RF Power and Efficiency. The efficiency and RF power for each diode are plotted in Figs. 2.7 and 2.8, respectively. From Eq. 2.18, the efficiency depends on V_{1N}, J_{1N} and θ_{1I} and hence its dependence on V_{1N} can be understood using the information of J_{1N} and θ_{1I} discussed previously. At small V_{1N}, the efficiency exhibits a quadratic dependence on V_{1N} because of the linear dependence of J_{1N} on V_{1N}. As J_{1N} saturates, the efficiency is linearly dependent on V_{1N}. After reaching its maximum, the efficiency drops and becomes negative due to significant changes in both J_{1N} and θ_{1I}. The GaAs Read diode has the highest decreasing rate in the efficiency, however the GaAs uniform diode has a lower decreasing rate than the other diodes, which is mainly due to the behavior of θ_{1I} in this diode.

The maximum efficiencies are 29.66 percent at V_{1N} = 0.71 for the GaAs Read diode, 21.84 percent at V_{1N} = 0.71 for the GaAs uniform diode, 26.37 percent at V_{1N} = 0.61 for the Si hybrid diode, and 26.98 percent at V_{1N} = 0.69 for the Si uniform diode. The GaAs Read diode shows the highest efficiency among all the diodes even though its J_{1N} is lower than that of any other diode. This results from the fact that the Read diode can achieve a larger voltage modulation ratio and phase delay in the fundamental current. It is interesting to note that the efficiencies of both GaAs and Si uniform diodes become negative when V_{1N} is greater than 0.9 due to the slowly varying property of θ_{1I} in both diodes.

The RF power vs. V_{1N} is plotted in Fig. 2.8. The RF power is the product of dc power and efficiency and therefore has a similar behavior except for some minor difference caused by the variation of dc power with V_{1N}.

4. Admittance and Impedance. The negative device conductance
and resistance are plotted in Fig. 2.9. As shown in the figure, both
decrease with increasing V_{1N}. The negative device conductance $- G_{d1}$,
as defined in Eq. 2.16, is dependent on $J_{1N}/V_{1N} \cos (\theta_{1I})$. Since
J_{1N} does not increase rapidly with increasing V_{1N}, the ratio
J_{1N}/V_{1N} is a decreasing function of V_{1N}. This is the reason why
$- G_{d1}$ always falls off. The rapid fall off in $- G_{d1}$ for the GaAs
Read diode at high V_{1N} results from the characteristic of its J_{1N}.
The difference in $- G_{d1}$ among diodes is attributed to the factor
J_{dc}/V_{dc}, shown in Eq. 2.16. The GaAs uniform diode has the highest
J_{dc}/V_{dc} so it has the highest $- G_{d1}$.

The device susceptance B_{d1} is defined as

$$B_{d1} = \frac{J_1 \sin (\theta_{1I}) + J_{dis}}{V_1} \qquad (2.24)$$

or

$$B_{d1} = \frac{J_1}{V_1} \sin (\theta_{1I}) + \omega C , \qquad (2.25)$$

where J_{dis} is a displacement current and C is a cold capacitance. The
second term on the right-hand side of Eq. 2.25 is always the dominant
term. The first term, which is contributed from the induced current,
is always negative because of the value of θ_{1I} and apparently decreases
in magnitude for increasing V_{1N} because of the property of J_{1N}/V_{1N}.
This results in an increasing behavior of B_{d1} with V_{1N}.

The device impedance is the inverse of device admittance. It
is obvious from the property of device admittance that the negative
device resistance is a decreasing function of V_{1N}, but the device
reactance increases in magnitude with V_{1N}.

As discussed previously, the device fundamental properties are dependent on the behavior of the fundamental current with RF voltage. A significant fall off in the fundamental current magnitude has been observed for each diode investigated. This fall off results in a decrease in efficiency and RF power. The reason for the fall off is discussed later.

2.3.3b Harmonic Current Generation. The device nonlinearity can be understood through the calculation of the harmonic currents in the diode. For the sake of cost and accuracy, only the first two harmonic currents are calculated. It is convenient to denote $\tilde{J}_m$ for the mth harmonic current phasor, where $m = 2,3,\ldots.$ The magnitude and phase angle of the phasor are denoted by J_m and θ_m, respectively. The characteristics of J_{mN} (defined as $J_{mN} = J_m/J_{dc}$) and θ_m are illustrated in Figs. 2.10 and 2.11.

According to the Bessel inequality,[78]

$$\frac{1}{2} (J_1^2 + J_2^2 + J_3^2) \leqq \frac{1}{2\pi} \int_0^{2\pi} |J_{ind}|^2 \, d\omega t - J_{dc}^2 \quad . \qquad (2.26)$$

Dividing both sides of Eq. 2.26 by J_{dc}^2 yields

$$\frac{1}{2} (J_{1N}^2 + J_{2N}^2 + J_{3N}^2) \overset{\leq}{=} \frac{1}{2\pi} \int_0^{2\pi} \left|\frac{J_{ind}}{J_{dc}}\right|^2 \, d\omega t - 1 \quad . \qquad (2.27)$$

Equation 2.27 indicates that there is an upper limit for J_{mN}, which depends on the induced current waveform. From simulation results, the maximum achievable values of J_{2N} and J_{3N} are found to be 2.2 for the Si uniform diode and 1.3 for the GaAs uniform diode. Both values are higher than that of J_{1N}. In other words, in terms of harmonic current generation, both diodes seem to be very nonlinear in single-frequency operation.
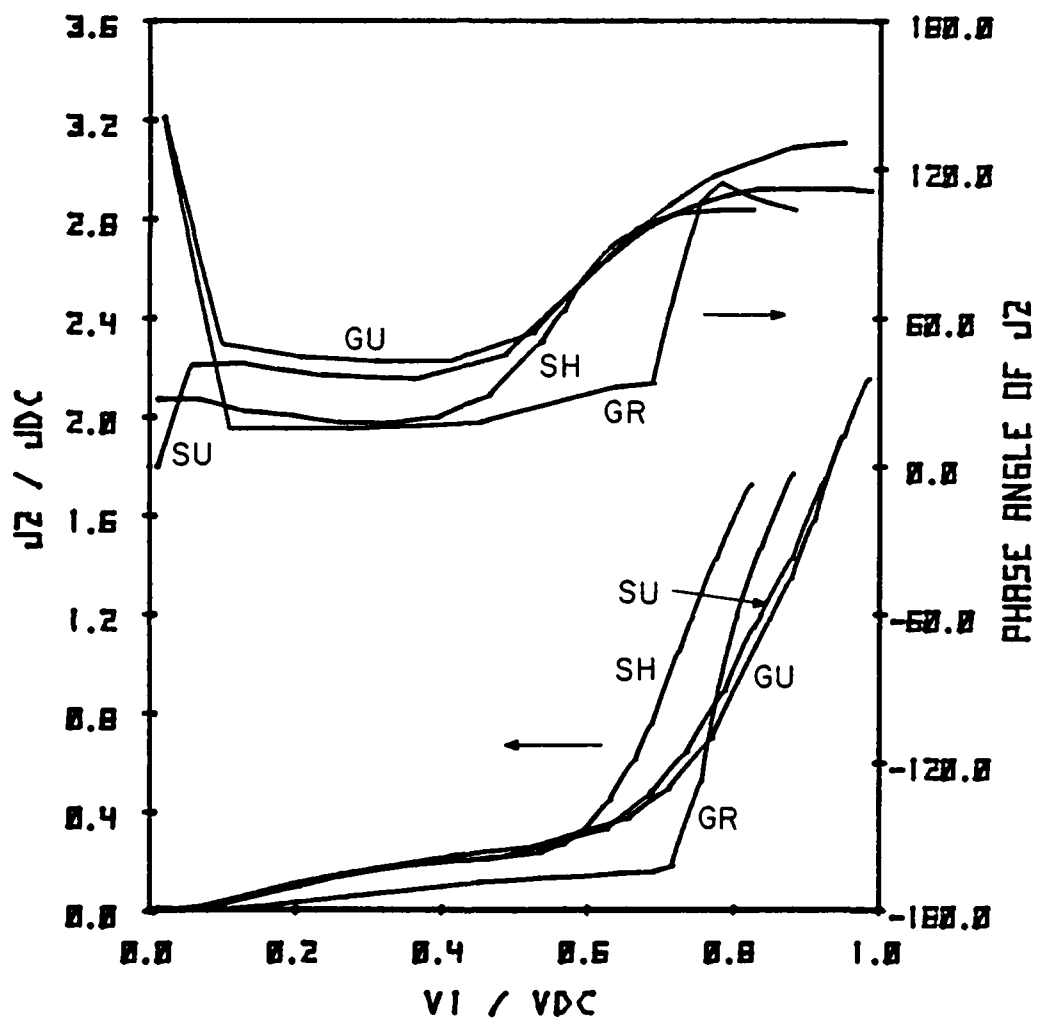
FIG. 2.10 NORMALIZED SECOND-HARMONIC CURRENT AND ITS

PHASE ANGLE VS. NORMALIZED FUNDAMENTAL VOLTAGE.

-56-
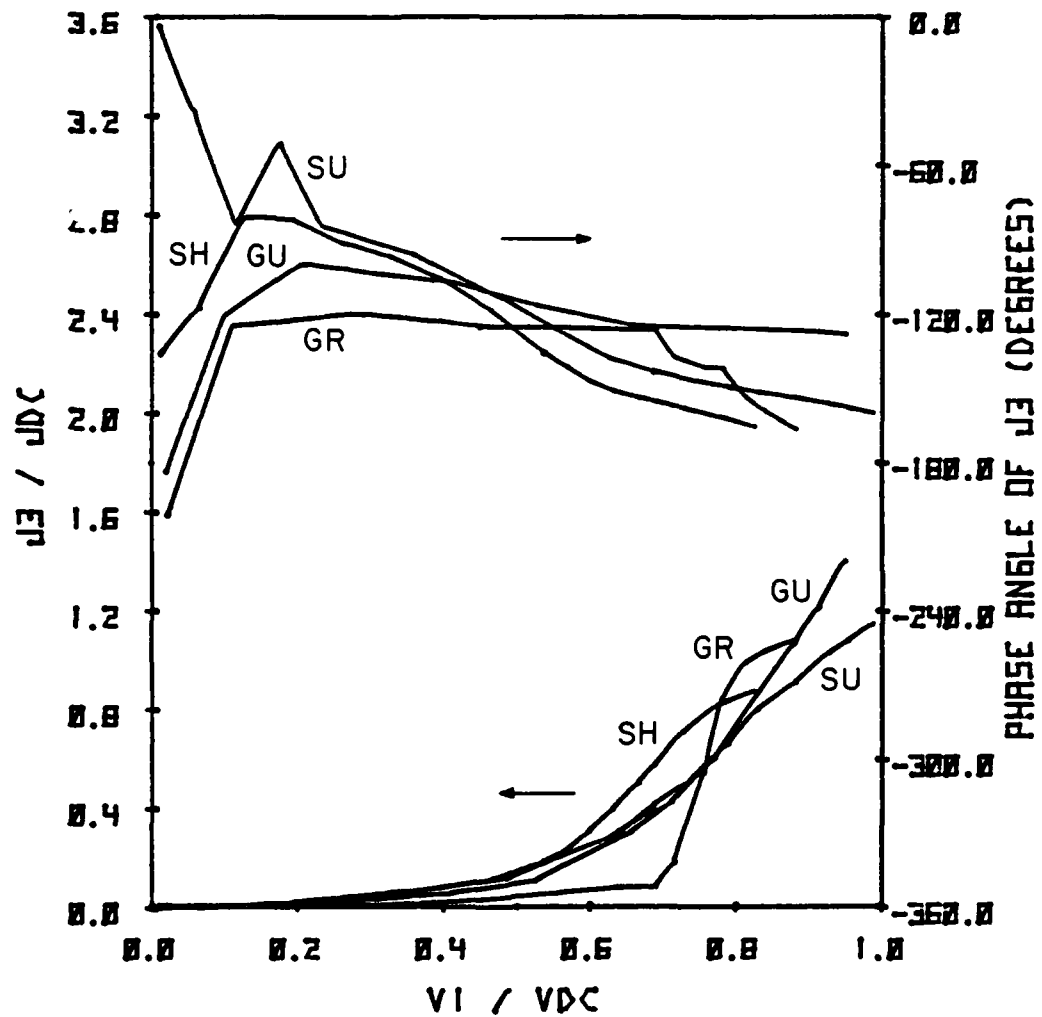
FIG. 2.11   NORMALIZED THIRD-HARMONIC CURRENT AND ITS PHASE

ANGLE VS. NORMALIZED FUNDAMENTAL VOLTAGE.

From Fig. 2.10 it is seen that for V_{1N} ranging from zero to
0.4, all J_{2N} curves, except those for the GaAs Read diode, are the
same and have a low increasing rate with V_{1N}. In this range, the
GaAs Read diode has a lower second-harmonic current than other diodes.
The reason is partly due to the longer transit time in this diode.
Until V_{1N} approaches V_{1NP}, J_{2N} is less than 0.3. After V_{1N} exceeds
V_{1NP}, the second-harmonic current for the GaAs Read and Si hybrid diodes
rises rapidly, but the current for the other two diodes increases
gradually at nearly the same rate.

Also shown in Fig. 2.10 is the second-harmonic current phase
angle θ_{2I} as a function of V_{1N}. The fast change in θ_{2I} at very low
V_{1N} (1 V) is because the large-signal simulation cannot give a
solution at low V_{1N} as accurately as at high V_{1N}. It is observed
from the figure that θ_{2I} tends to flatten at low V_{1N}, increases as
J_{2N} has a significant change, and finally flattens again at high
V_{1N}. For the GaAs Read and Si hybrid diodes, θ_{2I} approaches almost
the same value (103.1 degrees) at high V_{1N}; for the GaAs uniform diode,
θ_{2I} at high V_{1N} is approximately 131 degrees, which is higher than
that of other diodes.

In Fig. 2.11, at low V_{1N} the Si diodes exhibit the same
behavior in J_{3N} and have better harmonic current generation than the
GaAs diodes, but the value of J_{3N} is still low. However, at high
V_{1N}, J_{3N} rises. It can be observed that the GaAs uniform diode
has higher third-harmonic current generation than other diodes that
show signs of saturation in J_{3N}. This implies that the GaAs uniform
diode is more nonlinear in terms of third-harmonic current generation.
Despite the saturation behavior and magnitude difference, J_{3N} varies

in a manner similar to the corresponding J_{2N}. It can be seen from the figure that θ_{3I} decreases as V_{1N} increases, and θ_{3I} has a low decreasing rate for GaAs and Si uniform diodes. At high V_{1N}, θ_{3I} for the GaAs uniform diode will approach $- 120$ degrees, compared with the value around $- 160$ degrees for other diodes. This difference has a significant effect on diode performance in multifrequency operation. A detailed discussion is given later.

In conclusion, harmonic current generation for diodes is improved at high RF voltages. The phasors $\tilde{J}_2$ and $\tilde{J}_3$ increase in magnitude with RF voltage but rotate in the phasor plane in different directions. At high RF voltages, $\tilde{J}_2$ usually stays in the first quadrant and $\tilde{J}_3$ is in the second quadrant. This information is very important for harmonic power generation in multifrequency operation.

2.3.3c Effects of Avalanche Multiplication and the Drift Process.

From the simulation results presented in the previous section, it is seen that IMPATT diodes exhibit different behavior between low and high RF voltage regions. To study the related mechanisms responsible for the difference in behavior and to give a qualitative explanation are the purposes of this and the following sections. This section focuses on the effect of avalanche multiplication and the drift process on current generation.

Avalanche multiplication, which is an essential mechanism for injected current generation in IMPATT diodes, strongly depends on the ionization rates of carriers. It is known that ionization rates are highly nonlinear functions of electric field intensity and are different for different materials. As shown in Fig. 2.2, the ionization rates in both Si and GaAs increase rapidly with electric

field; however, they saturate at high electric fields. The saturation
behavior in ionization rates can be observed clearly from Fig. 2.12,
which plots α' vs. the reciprocal of electric field, by the fact that
α' (the derivative of ionization rate with respect to electric field)
goes down for electric fields greater than 0.5 MV/cm. The electron
ionization rate in Si shows a sign of saturation at an electric field
of approximately 0.8 MV/cm, as compared with a value of 0.5 MV/cm for
GaAs. The simulation results indicate that the maximum instantaneous
electric field in Si diodes at the highest driving condition is less
than 0.7 MV/cm and in GaAs diodes the maximum electric field is
approximately 0.8 MV/cm. Therefore, in normal operation, the Si
diodes will not experience saturation in ionization rates but the
GaAs diodes will. This gives rise to the difference in the injected
current waveform between both kinds of diodes and also the difference
in the back-bias voltage. Figure 2.12 indicates that GaAs has a nearly
zero α'' around E = 0.5 MV/cm, which is close to the critical dc electric
field in the GaAs Read diode. Hence, V_{bb} in this diode is very small
at small V_{1N}.

In general, the injected current J_{inj} is defined as the
following spatial integral:

$$J_{inj} = \frac{1}{w} \int_{-\frac{w}{2}}^{\frac{w}{2}} G(x,t) \, dx + J_n\left(x = -\frac{w}{2}, t\right) + J_p\left(x = \frac{w}{2}, t\right) \quad , \tag{2.28}$$

where w is the diode width and G is the generation rate. For qualitative
consideration, it is assumed that avalanche multiplication is localized
in a narrow avalanche region having a width of x_a, the carriers have
the same velocity, and the injected current is independent of position.
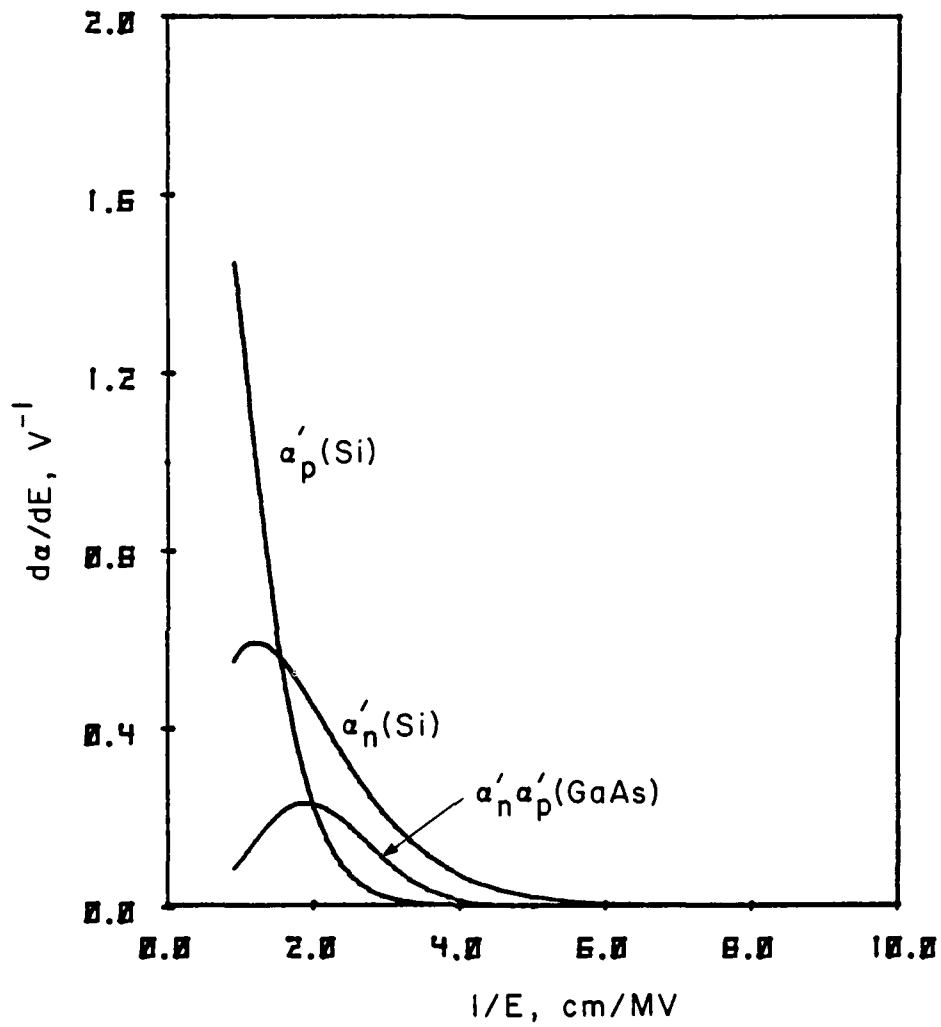
FIG. 2.12 dα/dE VS. RECIPROCAL OF ELECTRIC FIELD.

According to Misawa,[79] a differential form for J_{inj} can be obtained:

$$\frac{dJ_{inj}}{dt} = -\frac{J_{inj}}{M\tau_1} + \frac{J_s}{\tau_1} , \qquad (2.29)$$

where the multiplication factor M and intrinsic response time τ_1 are defined as

$$\frac{1}{M} = 1 - \int_{-\frac{x_a}{2}}^{\frac{x_a}{2}} \alpha_p \left[\exp \int_{-\frac{x_a}{2}}^{x} (\alpha_n - \alpha_p) \, dx \right] dx \qquad (2.30)$$

and

$$\tau_1 = \frac{1}{2v_s} \int_{-\frac{x_a}{2}}^{\frac{x_a}{2}} \left[\exp \int_{-\frac{x_a}{2}}^{x} (\alpha_n - \alpha_p) \, dx \right] dx . \qquad (2.31)$$

These two equations are derived assuming the avalanche region is symmetric about $x = 0$. It was also pointed out by Misawa that a rapid increase in the magnitude of $1/M\tau_1$ can be achieved provided that the dc electric field in a diode is in the region where non-saturated ionization rates are obtained and the fast change in $1/M$ results in a more pulse-like injected current, while the slow change leads to a more sinusoidal current. It can be expected that the Si diodes can produce sharper injected current waveforms than the GaAs diodes since the Si diodes operate in the nonsaturated region of the ionization rates, and the GaAs Read diode would have the worst injected current waveforms since the Read diode has a higher dc electric field than the other diodes. Figure 2.13 demonstrates the injected and induced current waveforms for the Si hybrid and GaAs Read diodes at their respective optimum RF

GAAS D-READ
JDC=1236 T=500
V=31,0,0 Q=0,0,0
FREQUENCY =   23.00 GHZ

SI HYBRID
JDC=1600 T=500
V=44 ,0,0 Q=0,0,0
FREQUENCY =   23.00 GHZ
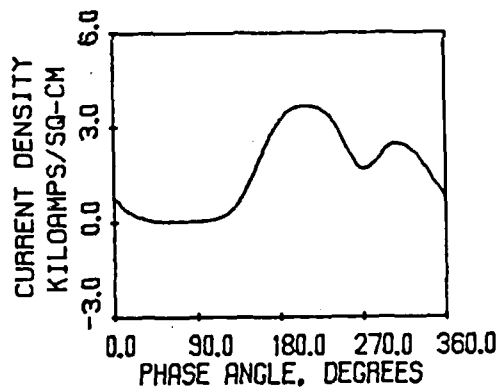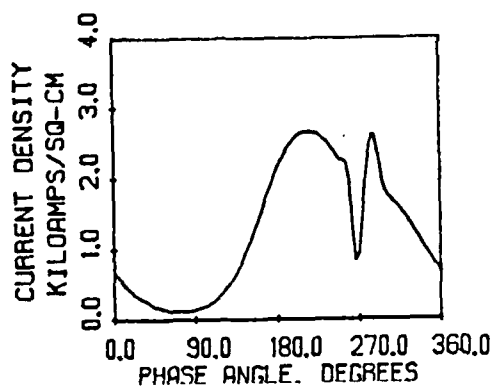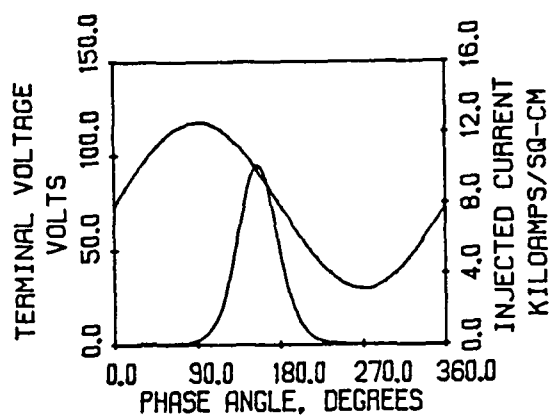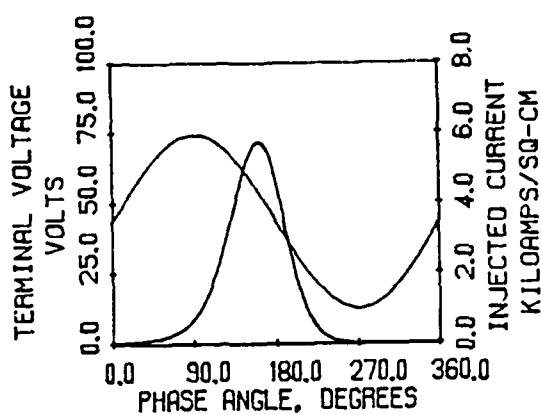
(a)

(b)

FIG. 2.13 LARGE-SIGNAL SOLUTIONS FOR (a) GaAs READ DIODE AT

V_1 = 31 V AND (b) Si HYBRID DIODE AT V_1 = 44 V.

voltages. It is seen from this figure that the injected current in the Si diode is sharp, compared with that in the GaAs diode.

In order to compare the injected current waveforms for the diode at various RF voltages, the ratio of the peak value of J_{inj} to J_{dc}, denoted as J_{injm}, and the width of J_{inj}, denoted as θ_ω, are plotted in Fig. 2.14. θ_ω is defined as the distance in the RF cycle between two points where the amplitude of J_{inj} is half of its peak value. This figure clearly illustrates that the GaAs Read diode has the worst current waveform under all the operating conditions, and the Si diodes have more peaked pulse-like current waveforms than the GaAs diodes. An interesting point is that all injected current waveforms tend to become more peaked as the RF voltage increases, but change slightly at high RF voltages. This implies that the back-bias effect plays an important role in the formation of the injected current, particularly at high driving conditions. Due to this effect, a reduction in dc voltage induced by an increase of RF voltage eventually will stop any further increase in the maximum instantaneous electric field in the diode, and avalanche multiplication will not increase proportionally with RF voltage. Therefore, no significant change in the current waveform can be observed at high RF voltages.

For a qualitative explanation of the observed fundamental and harmonic currents relative to the injected current, an analytic analysis similar to that in Chapter I is adopted. By assuming that carriers have the same property and the carrier spatial distribution remains undisturbed during transit and choosing the metallurgical junction of a double-drift IMPATT diode at the origin, the induced

-64-
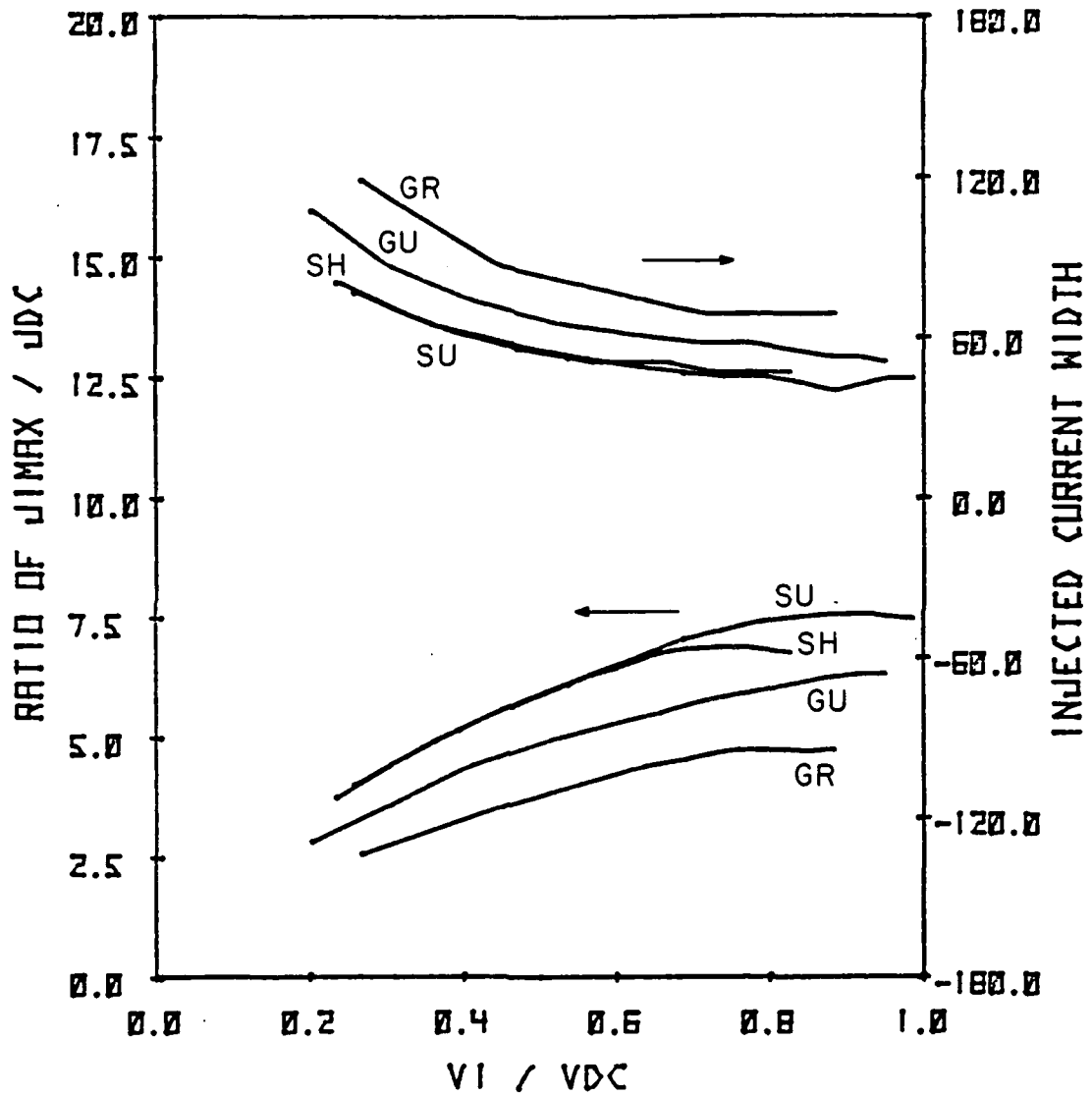
FIG. 2.14   RATIO OF THE PEAK VALUE OF INJECTED CURRENT TO dc

CURRENT DENSITY AND INJECTED CURRENT DENSITY WIDTH

VS. NORMALIZED FUNDAMENTAL VOLTAGE.

current can be written as

$$J_{ind} = \frac{1}{w}\left[x_a J_{inj} + 2 \int_{\frac{x_a}{2}}^{\frac{w}{2}} J_{inj}\left(t - \frac{x - (x_a/2)}{v_s}\right) dx\right] \quad, \quad (2.32)$$

where v_s is the drift velocity of a carrier. Based on simulation results, the injected current can be approximated by a bell-shaped function

$$J_{inj} = \frac{J_{dc}}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(\omega t - \theta_c)^2}{2\sigma^2}\right) \quad, \quad (2.33)$$

where θ_c is the center position of the injected current waveform and $\sigma = \theta_\omega/2.36$. (This expression is similar to the Taylor-expansion form of the current $J_{inj} = J_o \exp[-(V_a/2\tau_a)\cos(\omega t)]$ at $\omega t = 180$ degrees and neglecting higher-order terms.) Since the injected current drops quickly to zero for $|\omega t - \theta_c| < 3\sigma$, the Fourier series for the current can be written as

$$J_{inj} = \sum_{m=\infty}^{\infty} \frac{1}{2} \tilde{J}_{inj}^m e^{jm\omega t} \quad, \quad (2.34)$$

where $\tilde{J}_{inj}^m$ is the phasor of the mth harmonic of J_{inj} and is expressed as

$$\tilde{J}_{inj}^m = 2J_{dc} \exp\left(-\frac{m^2\sigma^2}{2}\right) \exp(-jm\theta_c) \quad. \quad (2.35)$$

Substituting Eq. 2.34 into Eq. 2.32 yields

$$J_{ind} = \frac{x_a}{w} \sum_{m=\infty}^{\infty} \frac{1}{2} \tilde{J}_{inj}^m e^{jm\omega t} + \sum_{m=\infty}^{\infty} \frac{v_s}{\omega} \frac{\tilde{J}_{inj}^m}{w} \theta_d \frac{\sin\frac{m\theta_d}{2}}{\frac{m\theta_d}{2}}$$
$$\cdot \exp\left(-j\frac{m\theta_d}{2}\right) e^{jm\omega t} \quad. \quad (2.36)$$

The normalized mth Fourier component of J_{ind} is defined as

$$\tilde{J}_{mN} = 2 \exp\left(-\frac{m^2\sigma^2}{2}\right)\left[\frac{x_a}{w} + \frac{2\theta_d}{\theta_a + 2\theta_d}\frac{\sin\left(\frac{m\theta_d}{2}\right)}{\frac{m\theta_d}{2}}\exp\left(-j\frac{m\theta_d}{2}\right)\right.$$

$$\left. \cdot \exp\left(-jm\theta_c\right)\right] \quad . \quad (2.37)$$

Assuming that x_a is small compared with w, J_{mN} is proportional to two factors $\exp(-m^2\sigma^2/2)$ and $\sin(m\theta_d/2)/(m\theta_d/2)$, that are plotted in Fig. 2.15. From Figs. 2.14 and 2.15 it is concluded that:

1. For a fixed θ_d, the fundamental current is expected to increase with decreasing θ_ω. According to the behavior of θ_ω shown in Fig. 2.14, the fundamental current is an increasing function of RF voltage or V_{1N} and tends to saturate when the RF voltage is high. This fact is in qualitative agreement with simulation results for the fundamental current shown in Fig. 2.4 for $V_{1N} < V_{1NP}$. The slightly higher fundamental current in the Si hybrid indicates that this approximate analysis cannot be applied well to the uniformly doped diode due to a spread of transit time for carriers. For higher values of RF voltage and from the preceding analysis, the fundamental current is expected to remain saturated; however, this is contrary to the fall off in the current indicated in Fig. 2.4a. This suggests that at high RF voltages, depletion-layer modulation should be taken into account. The effect of the modulation is discussed in the next section.

2. From Fig. 2.15 it is seen that the transit-time factor $\sin(m\theta_d/2)/(m\theta_d/2)$ is much lower in magnitude for harmonics for
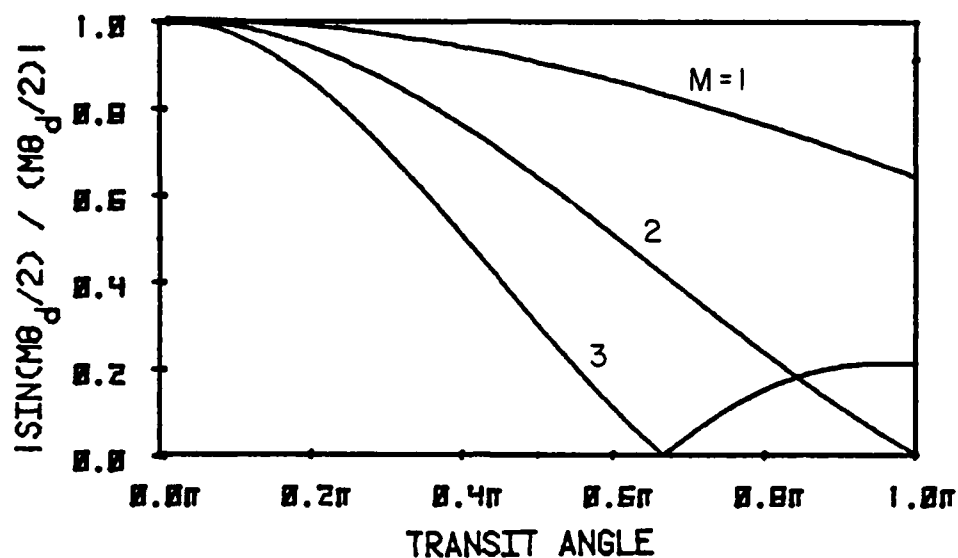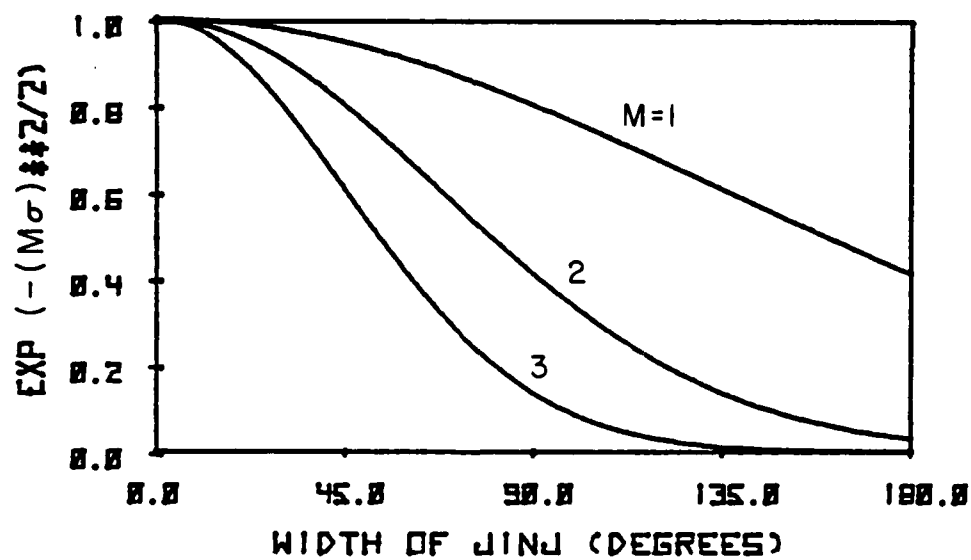
FIG. 2.15 (a) sin $(m\theta_d/2)/(m\theta_d/2)$ VS. THE TRANSIT ANGLE FOR

m = 1 TO 3 AND (b) exp $(-m^2\sigma^2/2)$ VS. THE WIDTH OF

THE INJECTED CURRENT FOR m = 1 TO 3.

the transit angle indicated in Table 2.2, but the other factor $\exp(-m^2\sigma^2/2)$ remains high. It is apparent that the drift process restricts harmonic current generation from the diodes. At low voltages, the increasing behavior of harmonic current with RF voltage is the direct consequence of the sharper injected current at higher RF voltages. At high voltages the rapid increase in the harmonic current is not attributed to the effect of avalanche multiplication and drift process, but the effect of depletion-layer modulation. Before depletion-layer modulation takes place, the overall harmonic current amplitude is so low that it is almost impossible to utilize the diodes for harmonic power generation at low RF voltages. In other words, the drift process is only advantageous for the fundamental power generation, not for harmonic power generation.

From Fig. 2.11 it is seen that Si hybrid and uniform diodes have almost the same harmonic current at low voltages, which is partly due to the same injected current width they have. The GaAs Read diode has the lowest harmonic current, which is definitely related to its worst injected current waveform.

2.3.3d Effects of Depletion-Layer Modulation. Depletion-layer modulation has been discussed by many researchers for its effects on the fundamental performance of an IMPATT diode. It can cause precollection of carriers[75] and modulation of carrier drift velocity. For a GaAs IMPATT diode with an appropriate doping profile, it can enhance the fundamental efficiency;[67] however, it is responsible for saturation of the fundamental efficiency in all diodes because of dissipation in an undepleted region.[80] In this section, the focus

is on its effects on the induced current waveform and harmonic current generation for the diodes investigated.

Depletion-layer modulation begins to occur when the RF voltage across a diode is high enough so that the electric field on either contact becomes negative at some point in the RF cycle. Without taking into account the back-bias effect, the threshold RF voltage level at which this modulation occurs is approximately 28.8 V for the GaAs Read diode, 21.25 V for the GaAs uniform diode, 33.25 V for the Si hybrid diode, and 31.96 V for the Si uniform diode. Up to this threshold level, the induced current waveform is roughly square in shape and out of phase with the RF voltage. Above this level, the current waveform undergoes a significant change and no longer has a square shape. This change produces a profound effect on device performance, particularly on harmonic current generation.

Basically, the depletion-layer modulation that occurs in an IMPATT diode is similar to that in a varactor diode that can be modeled by a nonlinear capacitance in series connection with a nonlinear resistance. The only difference between them is that the injected particles in an IMPATT diode affect the depletion-layer modulation and vice versa.

It is convenient to describe depletion-layer modulation in a single IMPATT diode rather than a double-drift IMPATT diode. The diode could be either a p-type or n-type Read diode. A schematic description for this modulation is illustrated in Fig. 2.16, which depicts the relative positions of the charge pulse and undepleted layer edge at three different phases corresponding to different driving conditions. For phase I shown in the figure, the charge pulse
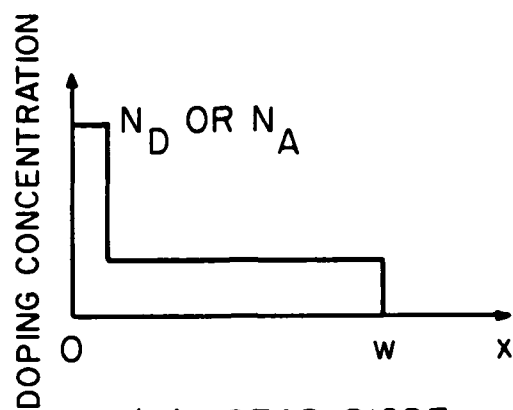
(a) READ DIODE
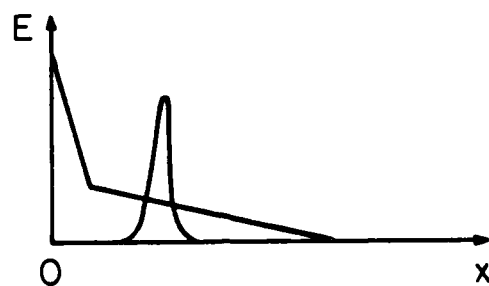
(b) PHASE I
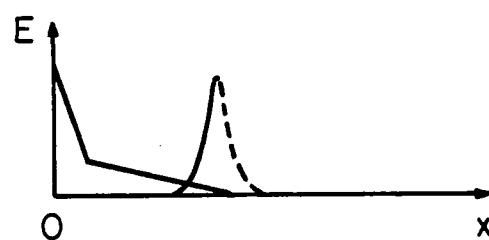
(c) PHASE II
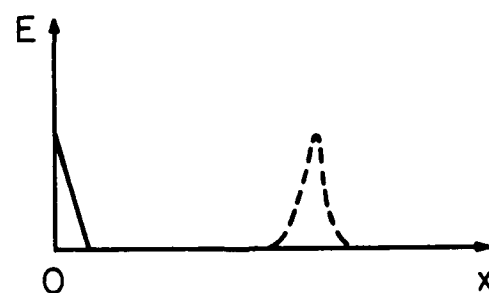
(d) PHASE III

FIG. 2.16   SCHEMATIC REPRESENTATION OF DEPLETION-LAYER MODULATION.

does not encounter the undepleted edge. For phase II, the charge pulse meets the undepleted edge. For phase III, the pulse has penetrated the undepleted region. Physically, modulation of the drift region requires flow of free charge carriers. When the undepleted layer edge moves inward, the charge carriers required to compensate the fixed impurity charge are supplied from an external current flowing through the contact, but the carriers drift velocity limits the rate of change of the undepleted region. The rate of change dw_n/dt should satisfy the following inequality:

$$\left|\frac{dw_n}{dt}\right| \leq v_{dmax} \quad , \tag{2.38}$$

where w_n is the position of the undepleted edge and v_{dmax} is the maximum drift velocity. This inequality is also held for the case in which carriers are extracted from the undepleted region. When the undepleted edge meets the charge pulse, the required charge carriers for compensation can be supplied partly from the charge pulse in addition to the external circuit, and dw_n/dt is limited by the ideal undepleted edge velocity.[67] This results in

$$\left|\frac{dw_n}{dt}\right| \leq \frac{\varepsilon}{qw_n N(w_n)} \left|\frac{dV_t}{dt}\right| \quad , \tag{2.39}$$

where N is the doping concentration at the undepleted edge. It is possible that in a low-doped diode the undepleted edge can move faster than the maximum drift velocity.

The phase I case is considered where no encounter occurs between the undepleted edge and the injected particles. Once a sinusoidal RF voltage exceeds a threshold value, the undepleted edge moves inward

prior to ωt = 270 degrees in the cycle. Before the electric field near the contact changes sign, the diffusion current flows first due to the large doping concentration gradient around the contact. After the electric field becomes negative, the drift current dominates the diffusion current in the undepleted region, but near the undepleted edge, the diffusion current is not negligible. The conduction current is now negative in the region. At ωt = 270 degrees, the undepleted region becomes wide and whether the conduction current is still flowing at this moment depends on the behavior of the electric field in this region. According to Eq. 2.39, dw_n/dt in the ideal case is zero at 270 degrees, and hence the electric field and conduction current vanish in the region. In a practical diode, the electric field cannot become zero immediately at 270 degrees, due to a delay process caused by the finite conductivity in the region. For ωt > 270 degrees, the electric field as well as the conduction current in the undepleted region gradually increase and become positive in order to remove the mobile carriers out of this region. The undepleted region reduces in width and finally disappears.

The terminal induced current density J_{ind} is defined as the average of spatial distribution of the conduction current density:

$$J_{ind} = \frac{1}{w} \int_0^w (J_n + J_p) \, dx \quad . \qquad (2.40)$$

The negative conduction current in the undepleted region prior to ωt = 270 degrees causes J_{ind} to decrease and thus J_{ind}, which depends on the v-E characteristic of carriers and the doping concentration, dips almost at 270 degrees. After ωt > 270 degrees,

J_{ind} increases because of the positive conduction current and reduction of the undepleted region width. It is concluded that depletion-layer modulation causes a dip in the induced current almost in phase with the voltage and makes the efficiency lower. However, the harmonic current is expected to increase because of the nonsinusoidal induced current waveform.

For phase II, the driving RF voltage is high enough to cause the undepleted edge to meet the charge pulse (injected particles) and carrier collection will take place. The carriers collected relax very quickly (of the order of a dielectric relaxation time) and a part of the free carriers needed to compensate the fixed impurity charge can be provided from the injected particles. Therefore, the induced current is expected to decrease significantly. The injected particle current affects the field near the undepleted edge as well as the velocities of carriers, particularly for the electron carriers in a GaAs diode. The case of a GaAs diode is considered in which the peak carrier density in the injected particles is somewhat higher than the background doping concentration. The field peaks around the center position of the injected pulse. This tends to bunch up the pulse as it is accelerated into the undepleted region and produce a spike of current near $\omega t = 270$ degrees. When the RF voltage recovers after $\omega t \stackrel{>}{=} 270$ degrees, the field increases and passes through the value for which the peak electron velocity is obtained. Therefore, mobile carriers in the undepleted region are extracted at velocities higher than the saturated velocity, producing the second broad peak in the induced current. More harmonic current can be generated in phase II.

For phase III, the RF voltage is much higher than that in the previous cases. Most carriers in the pulse are collected prior to $\omega t = 270$ degrees and the induced current becomes negative somewhere around $\omega t = 270$ degrees in the cycle, since only the negative conduction current exists in the diode. The diode at that moment is nothing different from a varactor diode. As before, when the electric field recovers in the undepleted region, the mobile carriers in the undepleted region are extracted at their respective maximum velocities. However, not all mobile carriers can be extracted at the end of the cycle and a significant amount of current flows at the beginning of the next cycle. This further reduces the fundamental efficiency, but, in accordance with the simple analysis in Chapter I, the induced current is rich in harmonic contact.

Depletion-layer modulation affects not only harmonic current generation but also back-bias voltage. For the diodes investigated, before the depletion-layer modulation occurs, the field in the avalanche region can have equal swings in both the positive and negative directions, but after the depletion-layer modulation occurs, the field has a larger swing in the negative direction than the positive one. This unequal field swing causes the dc voltage to drop further, particularly for the GaAs Read diode.

Due to the different v-F characteristics of electrons and holes and the different doping concentrations on both the n- and p-sides, the double-drift IMPATT diodes investigated have more complicated current waveforms than a single-drift diode. A detailed discussion based on simulation results is given next.
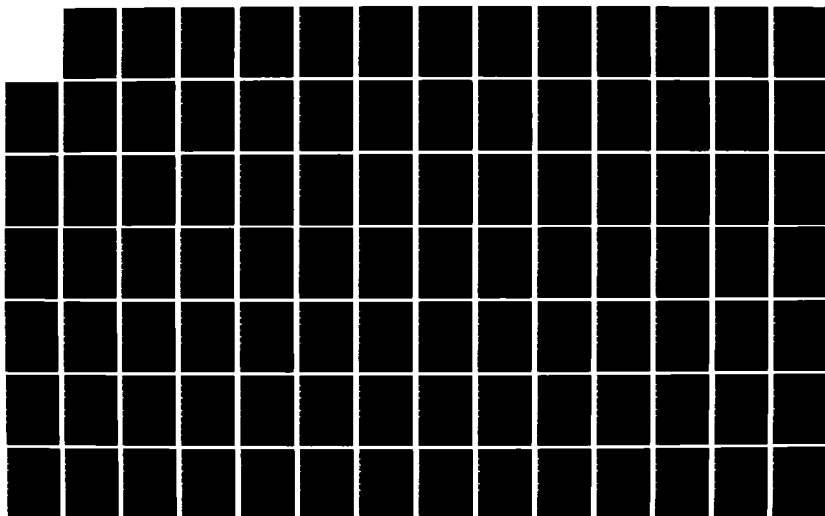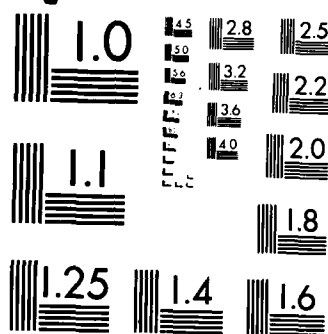
MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

The GaAs Read diode has a higher doping concentration in the p-side than on the n-side. According to the dc solution shown in Table 2.2, the field at the n-side contact is lower than at the other contact. Depletion-layer modulation occurs on the n-side first, when the RF voltage exceeds the threshold value. Figure 2.17 shows the electric field distribution and conduction current in this diode for V_1 = 31 V at three different times in the RF cycle, and Fig. 2.18a shows the corresponding terminal current and voltage waveforms.

At ωt = 252 degrees, the peak positions of the holes and electrons carrier pulses are approximately 0.4 μm to the left and right contacts, respectively. The instantaneous terminal voltage is not high enough to start the movement of the undepleted edge on the n-side. The field at the n-side contact is now 0.37 kV/cm; hence, no drift current can be observed except for diffusion current near the n-side contact. Even though the diffusion current is negative, the induced current shown in Fig. 2.18a rises a little because the low field causes the electron carriers to move faster.

At ωt = 270 degrees, as shown in Fig. 2.17b, the undepleted edge in the n-side moves to the left to meet the electron pulse peak, but no depletion-layer modulation occurs on the p-side. Some of the electron carriers are collected, while the hole pulse continues to drift toward the left contact for collection. The field at the n-side contact is now positive and has a value of 15.0 V/cm. The mobile carriers on the n-side depleted region are being extracted and therefore, a positive but low conduction current appears on the n-side depleted region. From Fig. 2.18a, it is seen that the induced current
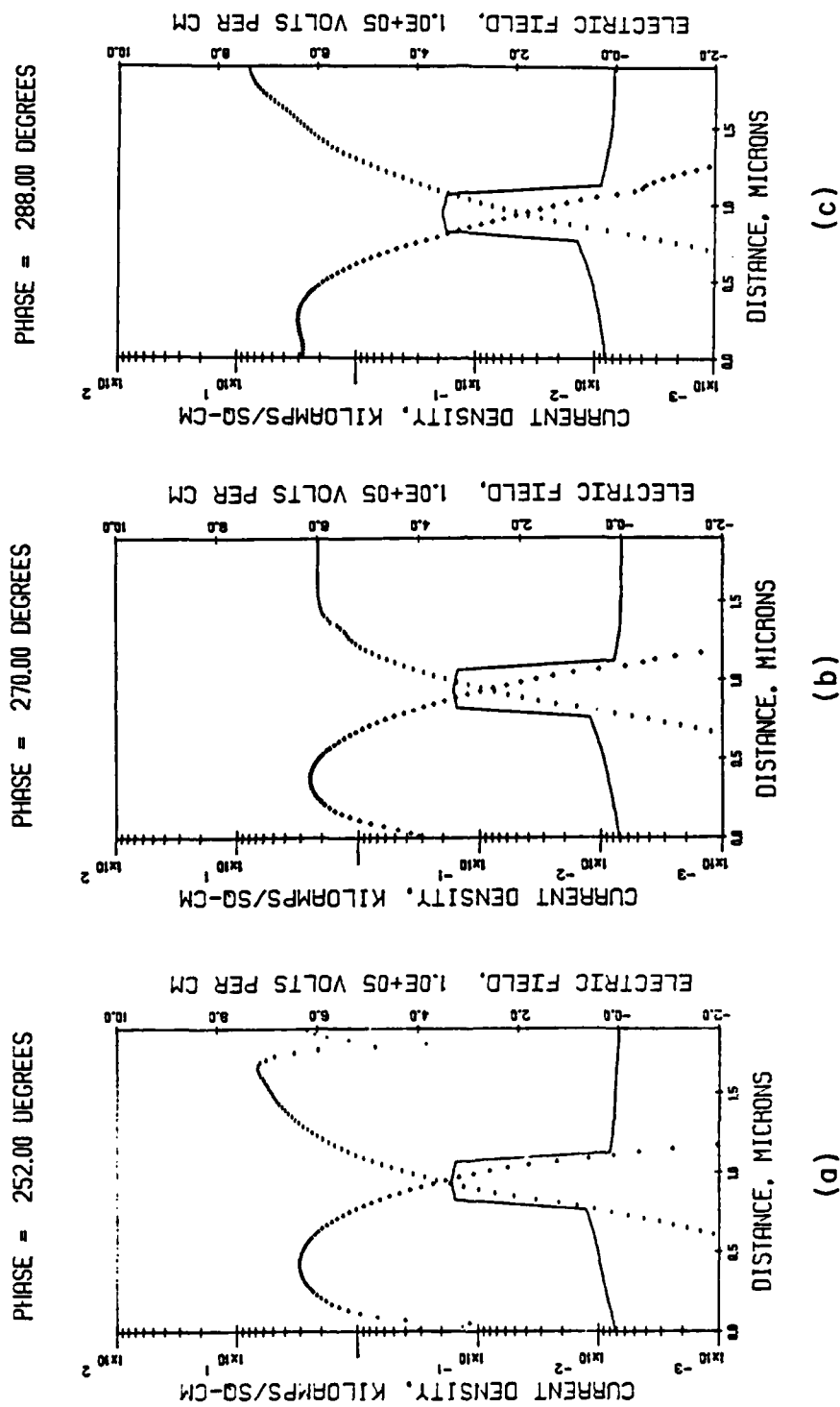
FIG. 2.17 STATES OF GaAs READ DIODE AT THREE DIFFERENT TIMES FOR V_1 = 31 V.

GAAS D-READ

JDC=1236 T=500

V=31,0,0 Q=0,0,0

FREQUENCY = 23.00 GHZ

GAAS D-READ

JDC=1236 T=500

V=32.6,0,0 Q=0,0,0

FREQUENCY = 23.00 GHZ

(a)

(b)
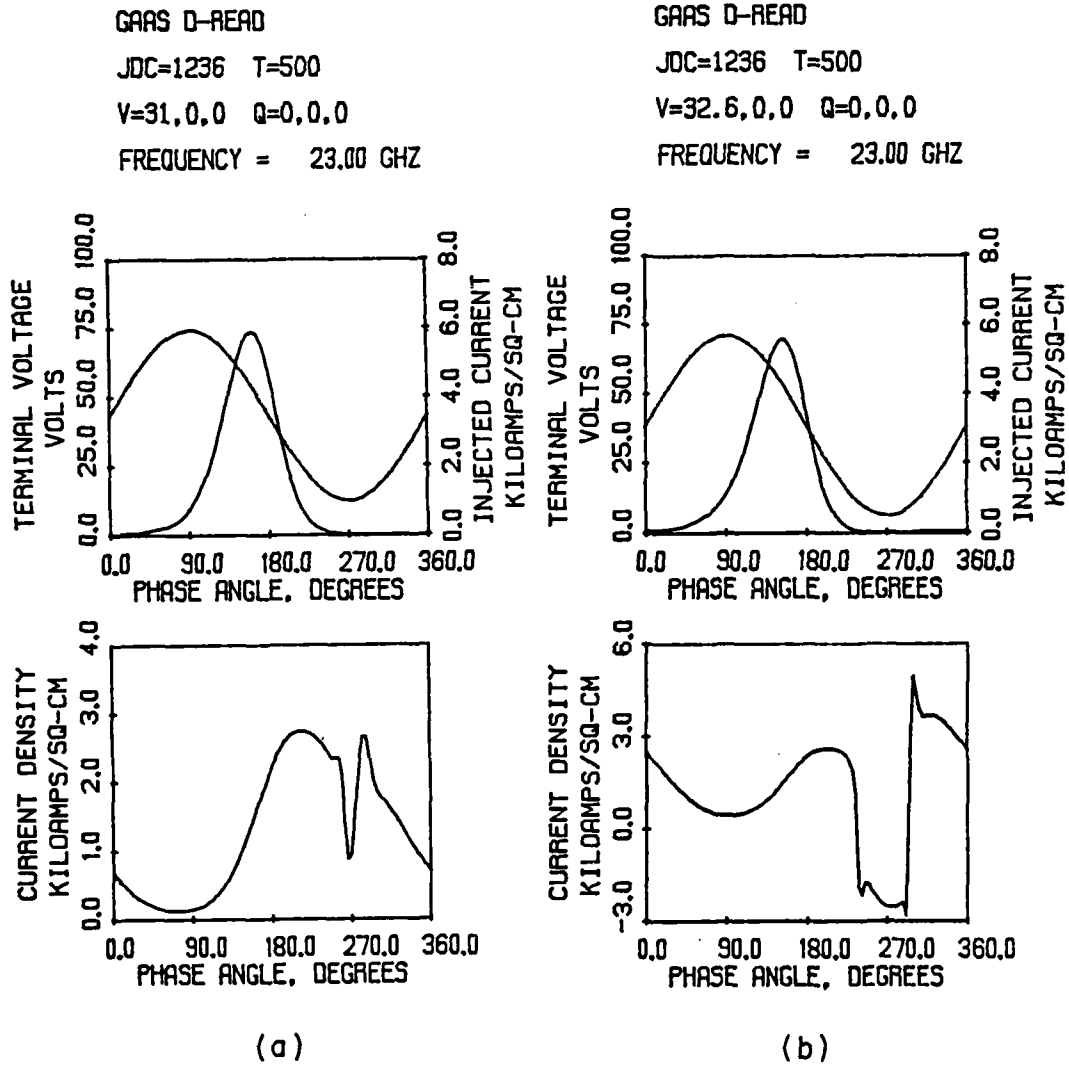
FIG. 2.18 LARGE-SIGNAL SOLUTIONS FOR GaAs READ DIODE IN

SINGLE-FREQUENCY OPERATION AT (a) V_1 = 31 V AND

(b) V_1 = 32.6 V.

starts to increase at this instant and dips slightly early at
$\omega t = 266.4$ degrees in the cycle.

At $\omega t = 288$ degrees, as shown in Fig. 2.17c, the field at the
n-side contact is 4.4 kV/cm and the electrons in the undepleted region
are extracted with a near peak velocity. Therefore, the conduction
current in the n-side depleted region is very large, producing a
spike in the induced current waveform. For $V_1 = 32.6$ V where the
efficiency is - 5.18 percent, the terminal current and voltage
waveforms are shown in Fig. 2.18b, and the conduction current and
field distribution at three instants in the cycle are shown in Fig.
2.19. At $\omega t = 234$ degrees, it is seen in Fig. 2.19 that the undepleted
edge on the n-side moves to the left to meet the electron pulse.
Because the field in the n-side undepleted region is - 4.4 kV/cm, which
is close to the critical field, a large but negative conduction current
is observed in this region. The induced current around this instant,
shown in Fig. 2.19a, drops sharply. However, the p-side undepleted
edge is still far from the hole pulse. As the terminal voltage
continues to decrease, the n-side undepleted edge encounters the
doping spike and almost stops moving. The negative field in the n-side
increases correspondingly and causes the negative conduction current
to decrease. Therefore, the induced current increases. As the
voltage decreases further, the p-side undepleted edge moves signi-
ficantly to cause the collection of the holes, so the induced
current decreases again. Around $\omega t = 270$ degrees, most of the hole
carriers have been collected and the negative fields in both undepleted
regions cause the mobile carriers in the regions to move at their
respective saturated velocities.
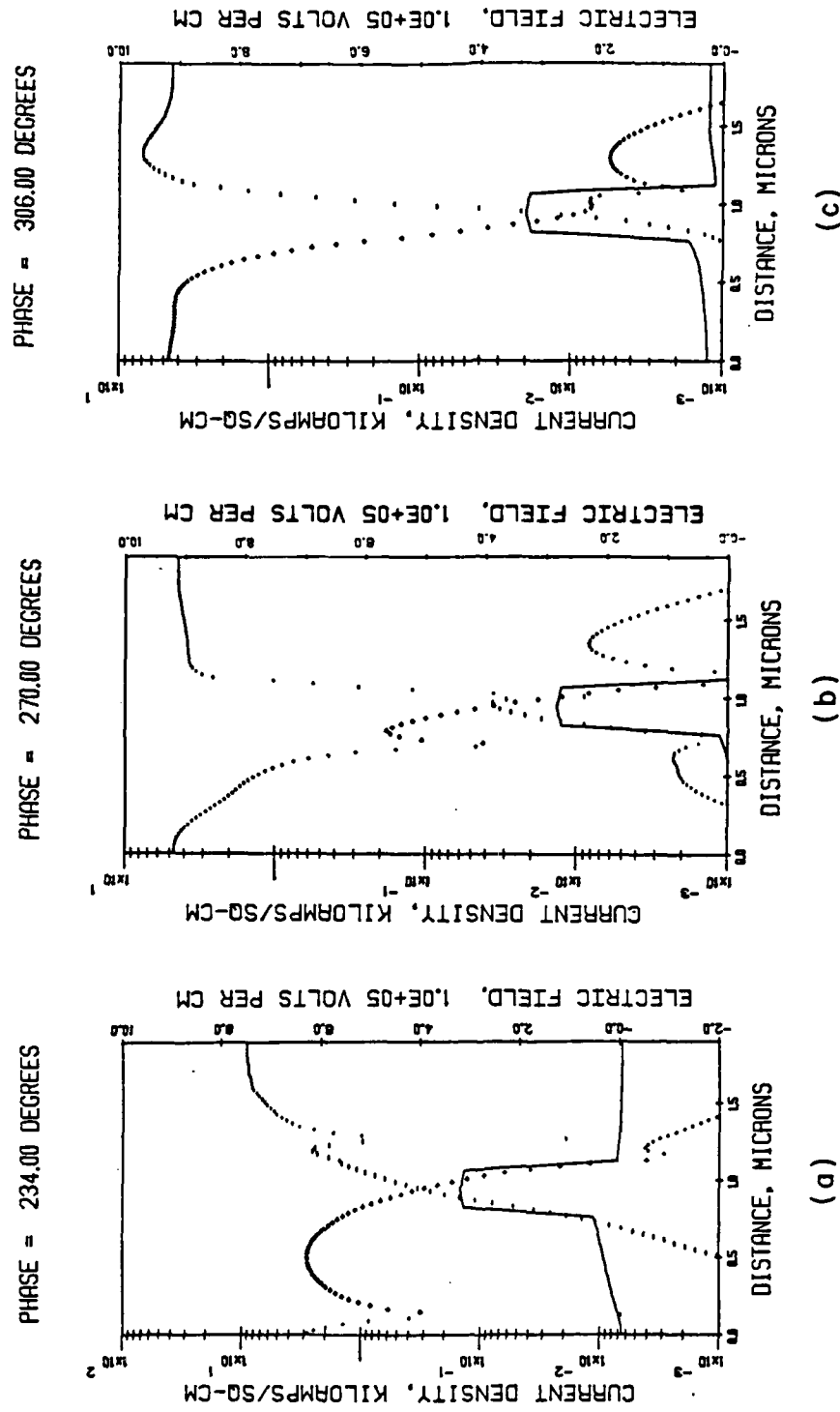
FIG. 2.19 STATES OF GaAs READ DIODE AT THREE DIFFERENT TIMES FOR V_1 = 32.6 V.

At ωt = 306 degrees, the terminal voltage recovers and the field in the n-side is positive and is higher than the critical field. The electrons are extracted at their saturated velocities. Similarly, the field at the p-side is approximately 2.5×10^4 V/cm and the holes are extracted at near saturated velocities. It is seen in Fig. 2.18b that the induced current is high but not maximum. Instead of a sharp dip, the induced current has a square shape. From simulation results, it is found that as the RF voltage increases to 33 V, the dip width increases but the current minimum changes slightly. This is why the harmonic current of this diode tends to saturate between V_1 = 32 and 33 V. It is concluded that the GaAs diode undergoes a rapid change in the induced current at high RF voltages because of the low doping concentration in the n-side and the v-E characteristic of electrons. This rapid change yields a sharp rise in harmonic current with RF voltage until saturation occurs.

The n-side of the Si hybrid diode has a doping concentration as low as that of the GaAs Read diode. The undepleted edge in the n-side can move fast, but the v-E characteristic of electrons in this diode makes it impossible for a sharp drop in the induced current to occur. Therefore, the harmonic current cannot rise as rapidly as that in the GaAs Read diode when the RF voltage increases. Figure 2.20a shows the induced current and terminal voltage waveforms at V_1 = 44 V, where the fundamental efficiency is maximum. It is seen that the induced current dips at ωt = 270 degrees, but not as sharply as that shown in Fig. 2.18a. Further simulation results indicate that the undepleted edges have a little movement without meeting the injected particles. This is equivalent to the case of phase I

SI HYBRID

JDC=1600 T=500

V=44 ,0,0 Q=0,0,0

FREQUENCY = 23.00 GHZ

SI HYBRID

JDC=1600 T=500

V=52 ,0,0 Q=0,0,0

FREQUENCY = 23.00 GHZ

(a)

(b)
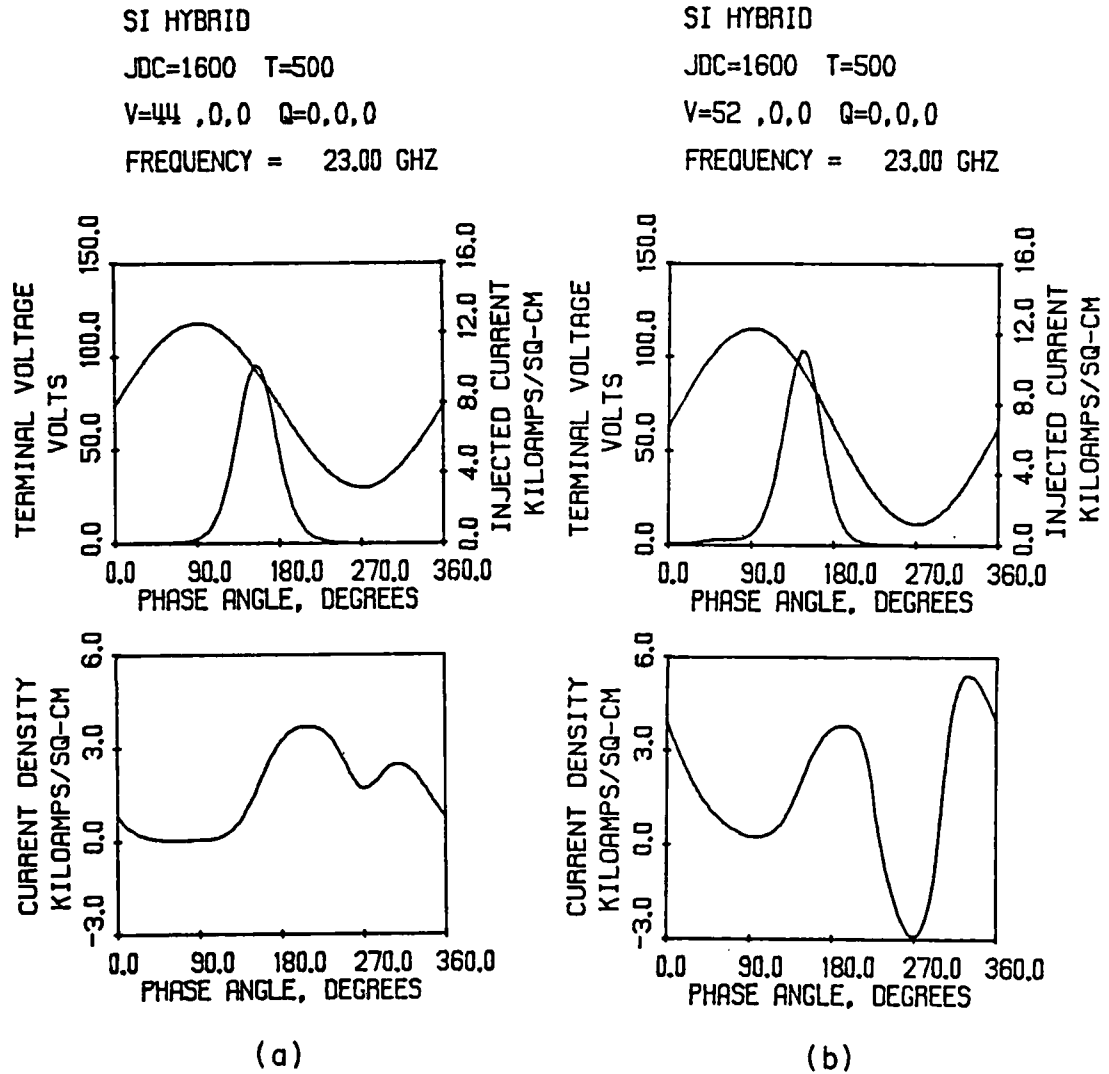
FIG. 2.20 LARGE-SIGNAL SOLUTIONS OF Si HYBRID DIODE IN

SINGLE-FREQUENCY OPERATION AT (a) V_1 = 44 V

AND (b) V_1 = 52 V.

mentioned before. The conduction current flowing in the undepleted

regions is restricted by the carrier mobilities in Si.

For $V_1 = 52$ V, where the fundamental efficiency is - 7

percent, the induced current shown in Fig. 2.20b dips significantly

at $\omega t = 270$ degrees and the current minimum is now - 2.93 kA/cm^2, which

is almost twice the dc current density in magnitude. The second peak

in the current appears at $\omega t = 327.6$ degrees, compared with $\omega t = 288$

degrees for the GaAs Read diode. The difference in the induced current

between the two diodes can be understood by referring to Fig. 2.21

which shows the field and conduction current in this Si diode at

three different instants in the cycle.

At $\omega t = 234$ degrees, the n-side undepleted edge moves close to

the highly doped region. It is noted that most of the injected

electrons have been collected. The undepleted region in this side

has an average electric field of - 30 kV/cm and a current density

of - 6.5 kA/cm^2. The p-side undepleted edge moves only 0.32 μm, which

is not enough to meet the hole pulse. The collection of electrons

causes the fall-off in the induced current around this instant, but

since the conduction current cannot rise as quickly as in the GaAs

Read diode, the fall off is not as significant as that shown in

Fig. 2.18b.

At $\omega t = 270$ degrees, the n-side undepleted region remains

unchanged and the field and current in this region increase slightly.

This region does not contribute to a further decrease in the induced

current. For the p-side, the undepleted edge moving to $x = 0.64$ μm

causes a slow collection of holes. Due to the v-E characteristic of

holes in this Si diode, the field only changes from - 26 kV/cm to

FIG. 2.21   STATES OF Si HYBRID AT THREE DIFFERENT TIMES FOR V_1 = 52 V.
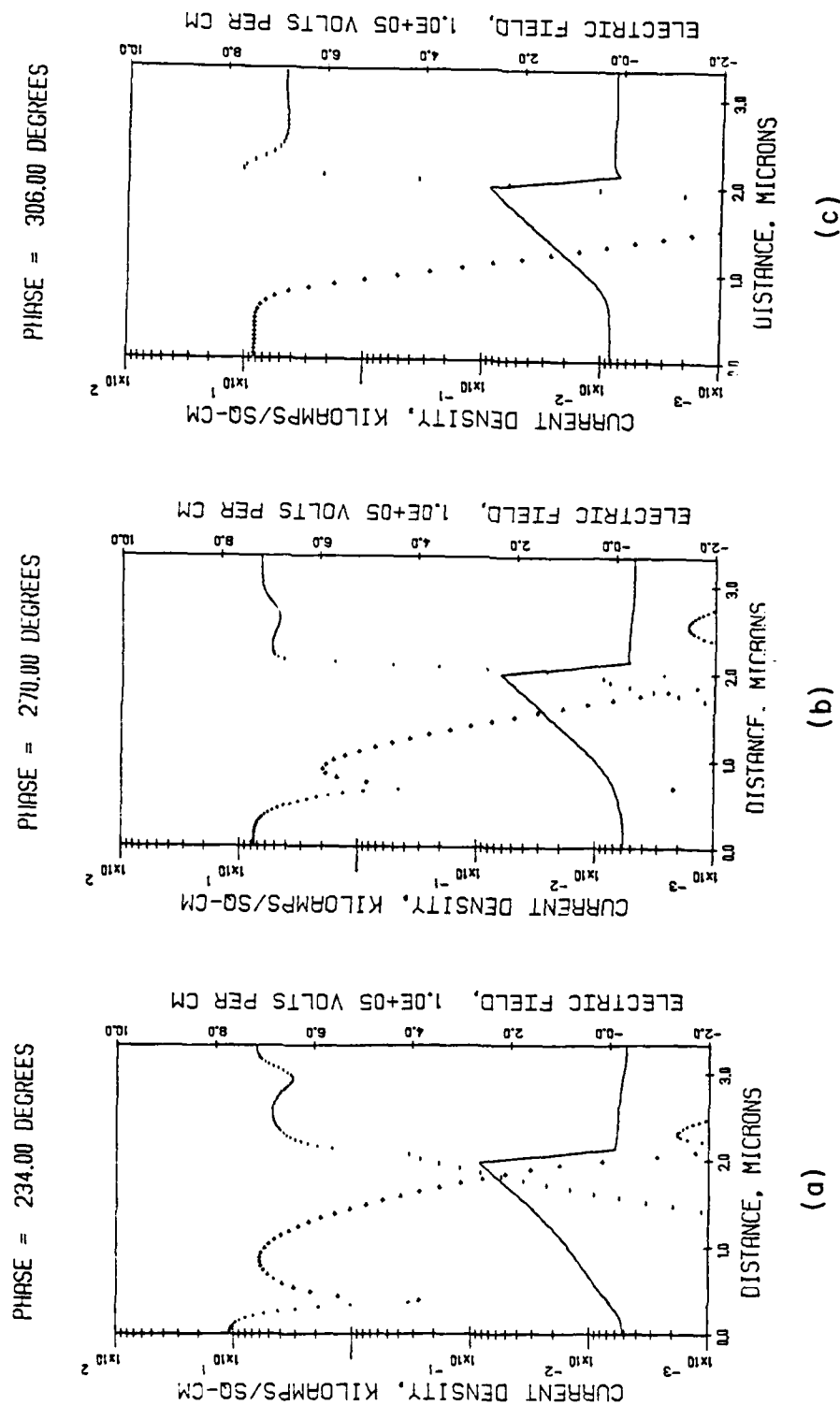
- 17 kV/cm and the corresponding conduction current changes from - 10 kA/cm^2 to - 7.3 kA/cm^2. These facts indicate that after the fall off in current caused by the collection of electrons, the induced current decreases gradually until ωt = 270 degrees. As a result, the harmonic current of this diode exhibits a sign of saturation around V_1 = 52 V.

At ωt = 306 degrees, the fields on both the p- and n-side contacts become 20 kV/cm and 16 kV/cm, respectively. Although these fields are not high enough to remove carriers at their respective saturated velocities, a considerable amount of conduction current flowing in each undepleted region can be observed from Fig. 2.21c. Consequently, the induced current rises, but not as rapidly as that in the GaAs Read diode due to the difference in the v-E characteristic of carriers between both diodes.

The Si uniform diode has higher doping concentrations on both sides than the previous two diodes. It is expected that both depleted edges will move slowly with decreasing terminal voltage, and the carrier collection process will slow down accordingly. Effects of high concentration on the induced current can be understood from Fig. 2.22. which shows the current and voltage waveforms for V_1 = 54 and 65.4 V. It is observed that the induced current dips gradually as the RF voltage increases, reaches its minimum at approximately 266.4 degrees in the cycle, and rises again in an almost similar manner as that in the Si hybrid diode. However, there are several differences in the current waveforms between both Si diodes: (1) The shape of the dip is always narrower in the Si uniform diode than in the Si hybrid diode. (2) Comparing the induced current waveforms for the Si

SI UNIFORM

JDC=2400   T=500

V=54 ,0,0   Q=0,0,0

FREQUENCY =   23.00 GHZ

SI UNIFORM

JDC=2400   T=500

V=65.4 ,0,0   Q=0,0,0

FREQUENCY =   23.00 GHZ

(a)

(b)
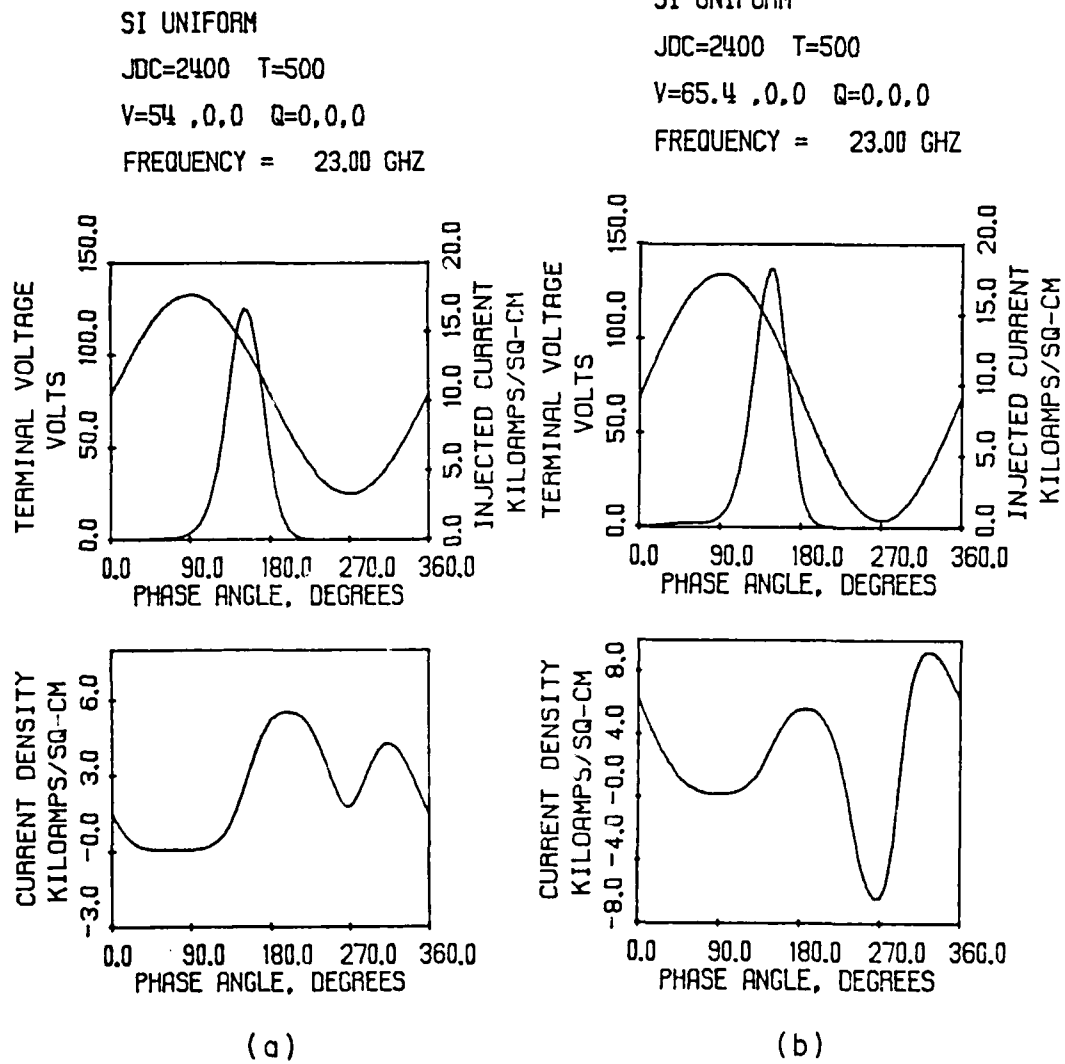
FIG. 2.22   LARGE-SIGNAL SOLUTIONS OF THE Si UNIFORM DIODE
IN SINGLE-FREQUENCY OPERATION AT (a) V_1 = 54 V
AND (b) V_1 = 65.4 V.

uniform diode at $V_1 = 65.4$ V and the Si hybrid diode at $V_1 = 52$ V (both diodes have the same efficiency at these points) shows that the current of the Si uniform diode has a minimum value of $- 6.5$ kA/cm^2, which is 2.7 times the dc current in magnitude, compared with a value of $- 2.9$ kA/cm^2 in the Si hybrid diode, which is only 1.8 times the dc current in magnitude. These differences result in higher harmonic current generation in the Si uniform diode. Since the induced currents of both diodes dip almost at the same instant in the cycle, the harmonic current phase angles of both diodes are nearly the same at higher voltages. Another point worth noting is that since the dip is narrower in the Si uniform diode, the fundamental efficiency will not become negative until the current minimum becomes very negative. It is concluded that high doping concentration improves harmonic current generation of the Si uniform diode.

The GaAs uniform diode has the highest doping concentration among the diodes investigated. Since the device length of this diode is almost one half that of the Si uniform diode, it is expected that harmonic current generation in this diode can be improved in a similar way as that in the Si uniform diode. The induced current waveforms of this diode, shown in Fig. 2.23, are similar to those shown in Fig. 2.22 except that the current waveform at $V_1 = 38$ V, shown in Fig. 2.23b, has a sharp peak at $\omega t = 288$ degrees in the cycle and the current dips at $\omega t = 255.6$ degrees which is significant. Since, in GaAs, the electron mobility is much higher than the hole mobility and the doping concentrations on both sides of this diode are not much different, the magnitude of electric field in the n-side undepleted region is much lower than that in the p-side and is

GAAS UNIFORM

JDC=3200 T=500

V=32 .0.0 Q=0.0.0

FREQUENCY = 23.00 GHZ

GAAS UNIFORM

JDC=3200 T=500

V=38 .0.0 Q=0.0.0

FREQUENCY = 23.00 GHZ

(a)

(b)
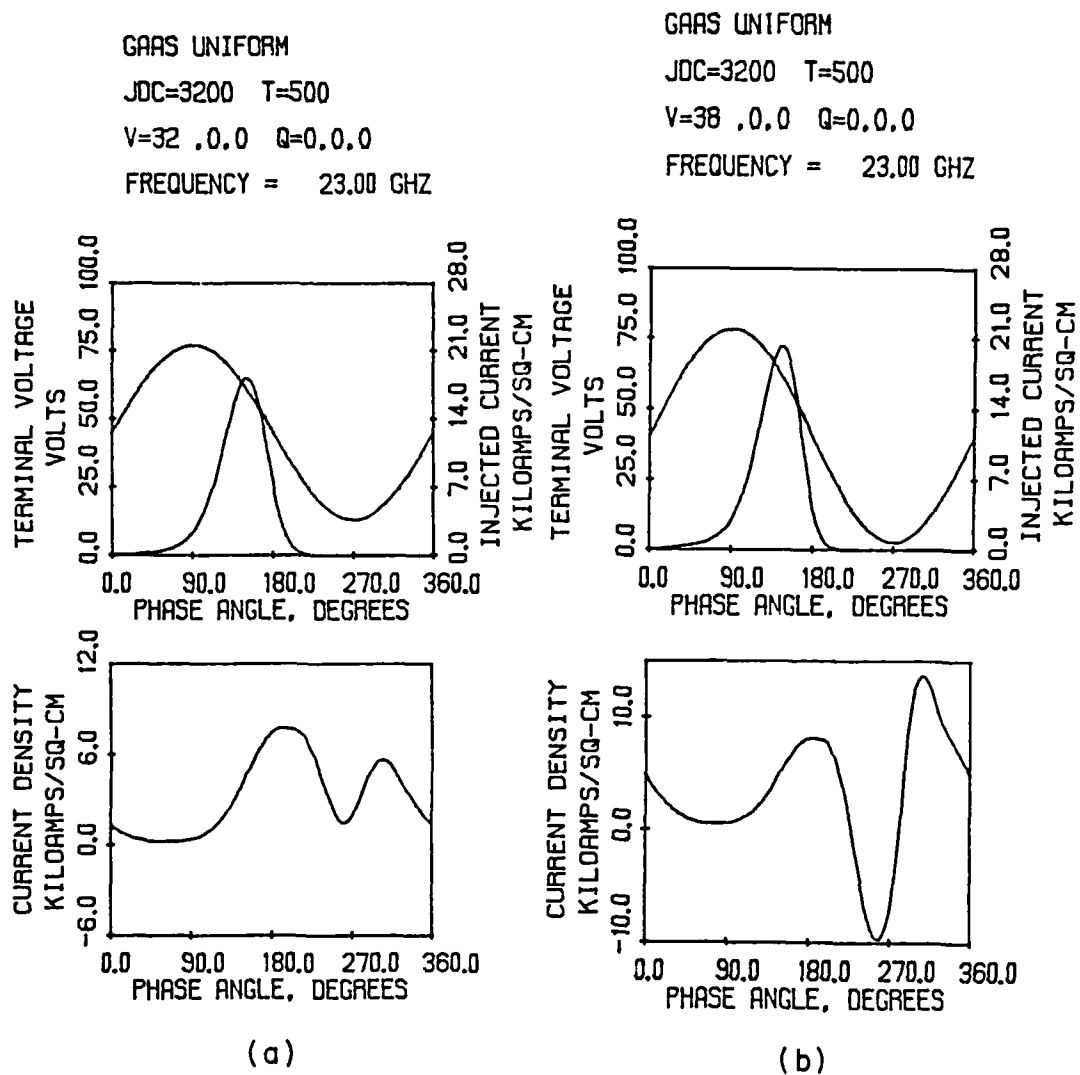
FIG. 2.23 LARGE-SIGNAL SOLUTIONS OF THE GaAs UNIFORM

DIODE IN SINGLE-FREQUENCY OPERATION AT (a) V_1 =

32 V AND (b) V_1 = 38 V.

usually less than the critical field (4 kV/cm) prior to $\omega t = 270$

degrees. As ωt approaches 270 degrees, the magnitude of the field

in this region decreases. This brings down the negative conduction

current significantly in this region. However, the current change

in the p-side undepleted region is small. Until $\omega t = 255.6$ degrees,

the decrease in the conduction current magnitude in the n-side

undepleted region becomes significant such that the induced current

stops decreasing, even though the undepleted regions continue to

widen. This unique property of the GaAs uniform diode gives the

following performance differences from the Si uniform diode:

1. Since the induced current of this diode dips not at $\omega t = 270$

degrees, the GaAs uniform diode can still have a positive fundamental

efficiency at $V_1 = 38$ V corresponding to $V_{1N} = 0.943$.

2. The induced current minimum at $V_1 = 38$ V is $- 9.73$ kA/cm^2,

which is over three times the dc current density.

3. The harmonic current phasor of the GaAs uniform diode always

leads those in the Si uniform diode at higher RF voltages.

2.3.3e Summary. In single-frequency operation, the

harmonic current generation of IMPATT diodes is subject to the effects

of avalanche multiplication, drift process, and depletion-layer

modulation. At low RF voltages, harmonic current generation depends

on the nonlinearity of the ionization rates but is degraded by the

drift process required to widen the induced current to achieve

optimum fundamental performance. Hence, the harmonic current ampli-

tude is much lower before the depletion-layer modulation takes

place. It is unlikely that diodes will be operated at low terminal

voltages to generate harmonic power.

Depletion-layer modulation leads to higher harmonic current generation. This modulation may be taken advantage of to generate harmonic power. However, the driving RF voltage should remain high enough to induce depletion-layer modulation significantly. Depletion-layer modulation is affected by doping profile and v-E characteristics of carriers. From the preceding discussion, it may be concluded that:

1. For GaAs Read and Si hybrid diodes, the low doping concentration leads to fast movement of the undepleted region edge with increasing RF voltage level; hence, it causes a rapid fall off in the fundamental efficiency and rapid increase in the harmonic current. The early collection of electron pulse is responsible for the saturation in the third-harmonic current. In general, the harmonic current of each diode is too sensitive to the change of the RF voltage level when depletion-layer modulation occurs.

2. For GaAs uniform and Si uniform diodes, the high doping concentrations on both p- and n-sides reduce the moving velocities of the undepleted region edges, hence, slowing down the carrier collection process. This makes the induced current dip gradually with increasing RF voltage and yields a harmonic current less sensitive to the change of RF voltage. Also, the fundamental efficiency does not drop as fast as that of the previous two diodes and becomes negative at very high voltage modulation. The v-E characteristic of electrons in GaAs makes the harmonic current phasor in the GaAs uniform diode lead that in the Si uniform diode. This has a significant effect on their harmonic power generation.

2.3.4 <u>Multifrequency Operation</u>. In multifrequency operation, device performance is determined by nonlinear interaction among the fundamental and harmonic voltages across the terminals. The presence of harmonic voltages yields a nonsinusoidal terminal voltage waveform that affects avalanche multiplication and depletion-layer modulation in a manner different from the single-frequency case. Consequently, the induced current waveform is modified considerably and so is the harmonic current content. It is the purpose of this section to investigate the effects of harmonic voltage on harmonic current generation and determine the optimum terminal voltage waveform to maximize the harmonic power output from the diodes. For simplicity, only one harmonic voltage is assumed to be present with the fundamental voltage across the terminals. A great deal of emphasis is placed on the third harmonic because of the interest in third-harmonic power combining.

2.3.4a <u>Third-Harmonic Performance</u>. In order to consider third-harmonic operation, the terminal RF voltage V_t is given by

$$V_t = V_1 \sin(\omega t) + V_3 \sin(3\omega t + \theta_{3V}) , \qquad (2.41)$$

where θ_{3V} is the phase angle of the third-harmonic voltage relative to the fundamental voltage. Normalizing V_t by V_1 yields

$$V_{tN} = \sin(\omega t) + V_{31} \sin(3\omega t + \theta_{3V}) ,$$

where $V_{tN} = V_t/V_1$ and $V_{31} = V_3/V_1$. In order to understand how the third-harmonic voltage modifies the terminal voltage waveform, the normalized terminal voltage waveform at $V_{31} = 1/9$ and 1/5 with θ_{3V} as a parameter ($\theta_{3V} = 0$, 30, 60 and 90 degrees) is plotted in Fig. 2.24. The choice of such θ_{3V} is based on the fact that the
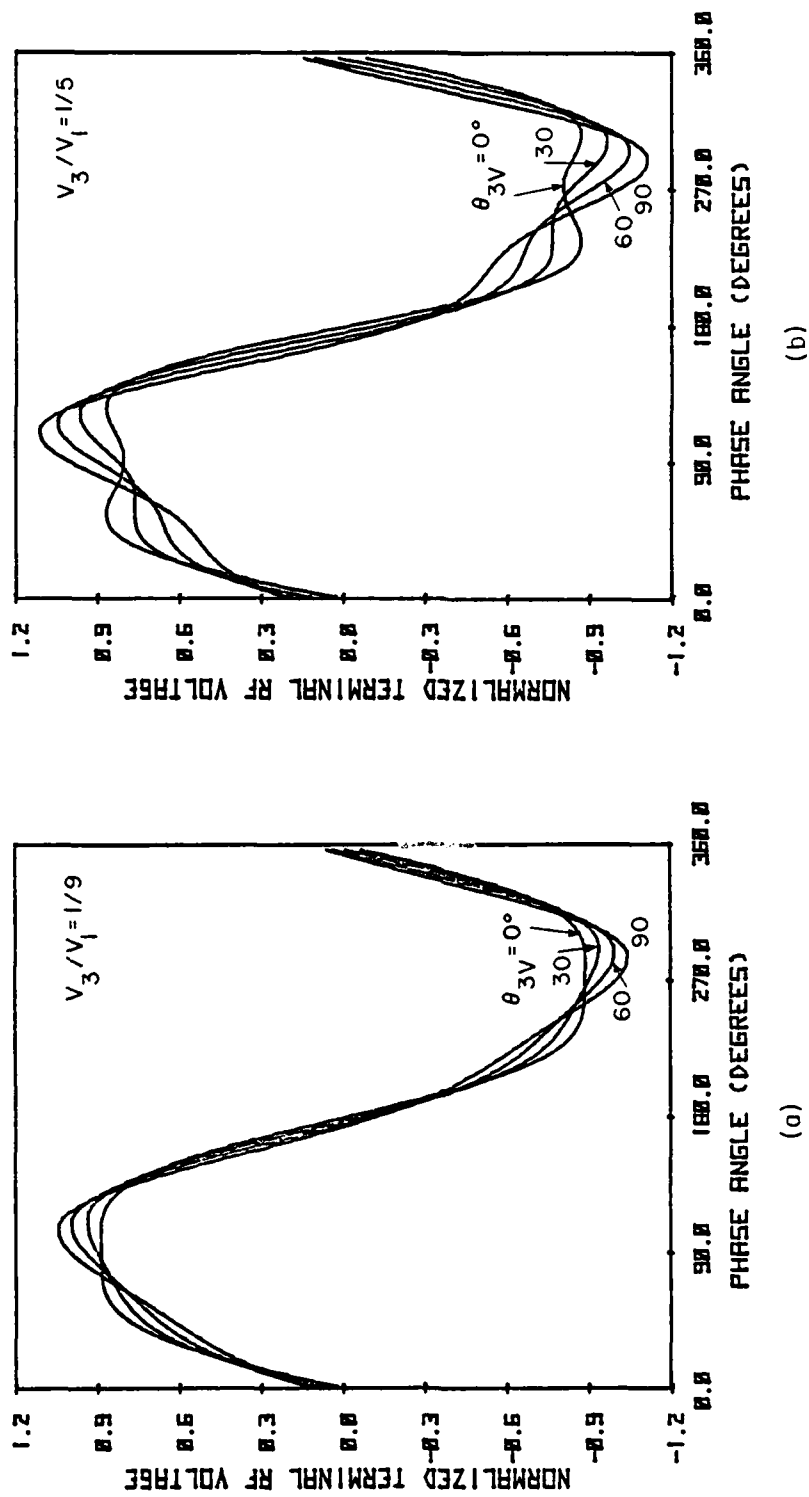
FIG. 2.24   PLOTS OF NORMALIZED TERMINAL RF VOLTAGE.   (a) $V_{tN} = \sin\theta + (1/5)\sin(3\theta + \theta_{3V})$

AND (b) $V_{tN} = \sin\theta + (1/9)\sin(3\theta + \theta_{3V})$.

third-harmonic current phase angle θ_{3I} at high RF voltages in single-frequency operation usually lies between $- 90$ and $- 180$ degrees. Therefore, in order to maximize the third-harmonic power output, θ_{3V} must be between zero and 90 degrees so that $\cos (\theta_{3V} - \theta_{3I})$ is closed to minus one.

The normalized terminal voltage at $V_{31} = 1/9$, shown in Fig. 2.24a has a unique negative peak. This is only true as long as V_{31} is less than one ninth. It is seen in the figure that the normalized voltage for $\theta_{3V} = 0$ degrees has a minimum value of $- 8/9$ at $\omega t = 270$ degrees in the cycle and becomes almost flat over a wide region around this point. In other words, the slope of the voltage is small around the voltage minimum point. As θ_{3V} increases the voltage minimum appears somewhere beyond $\omega t = 270$ degrees and shifts toward $\omega t = 270$ degrees with a more negative value. The voltage slope prior to the minimum point gradually increases in magnitude. The voltage for $\theta_{3V} = 0$ degrees becomes zero at $\omega t = 180$ degrees and this zero-crossing point shifts to the left of the point $\omega t = 180$ degrees as θ_{3V} increases. Since $V_{tN}(\omega t) = - V_{tN}(\omega t + 180)$, the voltage maximum has the same behavior as the voltage minimum except for the sign.

At $V_{31} = 1/5$, the normalized voltage shown in Fig. 2.24b has two minima for $\theta_{3V} = 0$ degrees, which are symmetrical on both sides of $\omega t = 270$ degrees and have the same value of $- 0.815$. It is seen in the figure that where θ_{3V} increases, the minimum appearing prior to $\omega t = 270$ degrees disappears gradually and, in contrast, the minimum appearing beyond $\omega t = 270$ degrees increases in magnitude and shifts its position toward $\omega t = 270$ degrees. The disappearance of the first minimum has a significant effect on the slope of the voltage

which can be observed in the figure. As before, the zero-crossing point shifts to the left of the point $\omega t = 180$ degrees when θ_{3V} increases.

For high V_1, the nonsinusoidal voltage waveform due to the presence of a third-harmonic voltage is expected to have the following effects on harmonic current generation:

1. For $V_3 \leq V_1/9$, depletion-layer modulation at $\theta_{3V} = 0$ degrees is suppressed due to a reduction in the negative minimum value in the terminal voltage. Consequently, the third-harmonic current is reduced. However, increasing θ_{3V} will enhance depletion-layer modulation and cause the third-harmonic current to increase. The dip in the induced current tends to shift to the right because it always appears close to the voltage minimum. This increases the phase delay of the third-harmonic current. Once the dip is not significant or shifts away from the fundamental voltage minimum, the fundamental efficiency increases and becomes more positive.

2. For $V_3 > V_1/9$, two voltage minima at $\theta_{3V} = 0$ degrees may make the undepleted edges move back and forth twice. Even though the voltage minimum prior to $\omega t = 270$ degrees disappears with increasing θ_{3V}, depletion-layer modulation is affected by variation in the slope of the voltage. Nevertheless, the induced current still dips near the other voltage minimum. As before, the third-harmonic current and its phase angle are modulated.

3. Particles are injected into a drift region early due to the left shift of the zero-crossing point of the voltage. Hence, they move farther into the drift region before depletion-layer modulation

takes place. This affects the carrier collection process and the dip shape in the induced current.

4. The injected current waveform may be modified in shape with varying θ_{3V} and V_3. This affects the third-harmonic current generation at low RF voltages.

5. The back-bias effect is modulated, depending on whether depletion-layer modulation is enhanced or suppressed. At $\theta_{3V} = 0$ degrees the back-bias effect is expected to decrease and, therefore, the dc voltage increases. For $\theta_{3V} > 0$ degrees, the enhancement in depletion-layer modulation makes the dc voltage decrease. Nevertheless, this gives a greater amplitude difference between the dc and the fundamental voltage. A higher harmonic voltage can be applied to the terminal without causing the diode to be forward biased.

In general, the third-harmonic current amplitude and phase angle are functions of V_1, V_3 and θ_{3V} and can be expressed as

$$J_3 = J_3(V_1, V_3, \theta_{3V}) \qquad (2.42)$$

and

$$\theta_{3I} = \theta_{3I}(V_1, V_3, \theta_{3V}) \quad . \qquad (2.43)$$

The normalized third-harmonic current amplitude J_{3N} is defined as

$$J_{3N} = J_3/J_{dc} \qquad (2.44)$$

and, therefore, the third-harmonic power and efficiency are given by

$$P_3 = -\frac{1}{2} V_3 J_3 \cos(\theta_{3V} - \theta_{3I}) \qquad (2.45)$$

and

$$\text{Eff}_3 = P_3/P_{dc} = -\frac{1}{2} V_{3N} J_{3N} \cos(\theta_{3V} - \theta_{3I}) \ . \qquad (2.46)$$

Active mode operation requires both Eff_1 and Eff_3 to be positive for power generation. Eff_3 can reach its maximum provided that the phase difference $\theta_{3V} - \theta_{3I}$ is approximately 180 degrees, but Eff_1 may not be positive in this situation. With fixed V_1 and V_3 and varying θ_{3V}, the following three cases are possible: (1) Eff_1 is always positive for all θ_{3V}, (2) Eff_1 becomes negative after Eff_3 reaches its maximum, and (3) Eff_1 becomes negative before Eff_3 reaches its maximum. For the first two cases, the maximum Eff_3 is chosen for comparison but for the last case, Eff_3 at $\text{Eff}_1 = 0$ is chosen for comparison. Details about harmonic current generation and maximum attainable third-harmonic efficiency for the diodes investigated are given next.

As discussed previously, the GaAs Read diode in single-frequency operation has a harmonic current that is sensitive to the variation of the RF voltage level. Consequently, the third-harmonic current undergoes a significant change while varying θ_{3V} and V_3. This can be understood by comparing the injected and induced current waveforms shown in Figs. 2.25 and 2.26 for $V_1 = 32.6$ V.

Without applying V_3, the injected current peaks at $\omega t = 154.8$ degrees in the cycle and has a peak value of 5.75 kA/cm^2 and a width of 68.4 degrees and the induced current shows a very broad dip around $\omega t = 270$ degrees. For $V_3 = 2$ V and $\theta_{3V} = 0$ degrees, the terminal RF voltage has a minimum value of -30.6 V, which is just low enough to cause depletion-layer modulation. A dip can be observed in the induced current waveform, shown in Fig. 2.25a, at $\omega t = 263$ degrees, but it is not significant. The injected current now has a peak value of
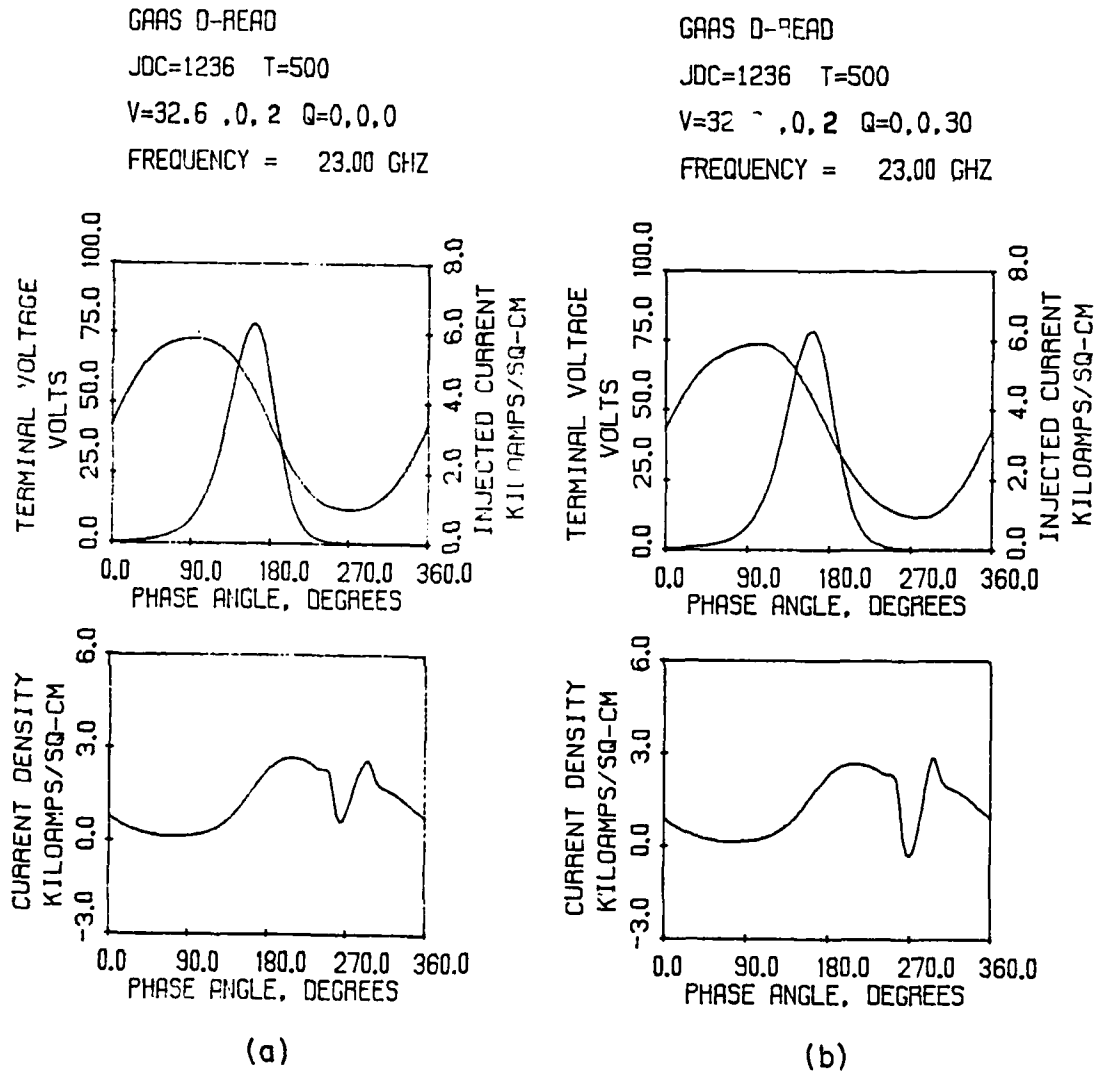
FIG. 2.25 LARGE-SIGNAL SOLUTIONS FOR THE GaAs READ DIODE AT

(a) V_1 = 32.6 V, V_3 = 2 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 32.6 V, V_3 = 2 V AND θ_{3V} = 30 DEGREES.

GAAS D-READ

JDC=1236 T=500

V=32.6 ,0.6 Q=0.0.0

FREQUENCY = 23.00 GHZ

GAAS D-READ

JDC=1236 T=500

V=32.6 ,0.6 Q=0.0.30

FREQUENCY = 23.00 GHZ

(a)   (b)

FIG. 2.26 LARGE-SIGNAL SOLUTIONS FOR THE GaAs READ DIODE AT

(a) V_1 = 32.6 V, V_3 = 6 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 32.6 V, V_3 = 6 V AND θ_{3V} = 30 DEGREES.

6.28 kA/cm^2 at $\omega t = 162$ degrees and a width of 64.8 degrees. This little improvement in the injected current has a negligible effect on the third-harmonic current due to the drift process. The third-harmonic current decreases from 1268 A/cm^2 to 326 A/cm^2 and the fundamental efficiency is improved from -4.9 to 30.27 percent. The decrease in the third-harmonic current indicates the essential role of depletion-layer modulation on the device nonlinearity.

Figure 2.25b shows the terminal voltage and current waveforms for $V_3 = 2$ V and $\theta_{3V} = 30$ degrees. The terminal RF voltage now has a negative peak value of -31.1 V at $\omega t = 278.5$ degrees. The increase in the negative peak value enhances depletion-layer modulation and causes the induced current to dip significantly at $\omega t = 270$ degrees. The third-harmonic current increases from 326 to 435 A/cm^2, and the corresponding Eff$_3$ changes from 0.48 to 0.84 percent. Although the injected current now has a narrower width of 61.2 degrees, it is believed that this narrow injected current contributes little to the increase in the third-harmonic current.

Figure 2.26 illustrates the terminal voltage and current waveforms for $V_3 = 6$ V. Since the corresponding V_{31} is now 0.184, which is greater than one ninth, the terminal RF voltage for $\theta_{3V} = 0$ degrees has two negative peaks with the same value of 28.27 V at $\omega t = 236.9$ and 303.1 degrees, respectively. It is clear from Fig. 2.26a that no significant depletion-layer modulation occurs for $\theta_{3V} = 0$ degrees, and only a small dip is observed at $\omega t = 303.1$ degrees, at which most carriers had been collected at the contact. As a result, the third-harmonic current is only 123 A/cm^2. Instead, avalanche multiplication plays a dominant role in determining the third-harmonic

current. However, the injected current width is now 68.4 degrees, which is still too wide to improve the third-harmonic current.

For $V_3 = 6$ V and $\theta_{3V} = 30$ degrees, as shown in Fig. 2.26b, the RF voltage negative peak becomes significant to enhance depletion-layer modulation to cause the induced current dip at $\omega t = 291.6$ degrees. Consequently, the third-harmonic current increases to 365.8 A/cm^2, but with more phase delay (184 degrees). It is seen from the phasor diagram shown in Fig. 2.27 that while the third-harmonic voltage rotates counterclockwise, the corresponding third-harmonic current rotates in an opposite direction with an increase in magnitude. This behavior reduces the phase difference $\theta_{3V} - \theta_{3I}$ and finally makes the third efficiency decrease.

Detailed effects of the third-harmonic voltage on device performance at $V_1 = 32.6$ V are shown in Fig. 2.28 which plots J_{3N} and Eff_3 as functions of θ_{3V} with V_3 as a parameter. It is seen in the figure that J_{3N} for $\theta_{3V} = 0$ degrees decreases significantly as V_3 increases from 1 to 2 V. The decrease in J_{3N} slows down for $V_3 \geqq 2$ V, and until $V_3 \geqq 4$ V, no significant decrease can be observed. This evidence is enough to indicate the sensitive dependence of depletion-layer modulation on the terminal RF voltage. At high V_3, with $\theta_{3V} = 0$ degrees, depletion-layer modulation is not significant and therefore the avalanche multiplication and drift process become important for third-harmonic current generation. However, J_{3N} is unfortunately small in this situation due to the drift process.

As θ_{3V} increases, J_{3N} increases accordingly due to the enhancement in depletion-layer modulation. It is clear from Fig. 2.28 that the increasing rate of J_{3N} is higher at higher V_3, since the RF
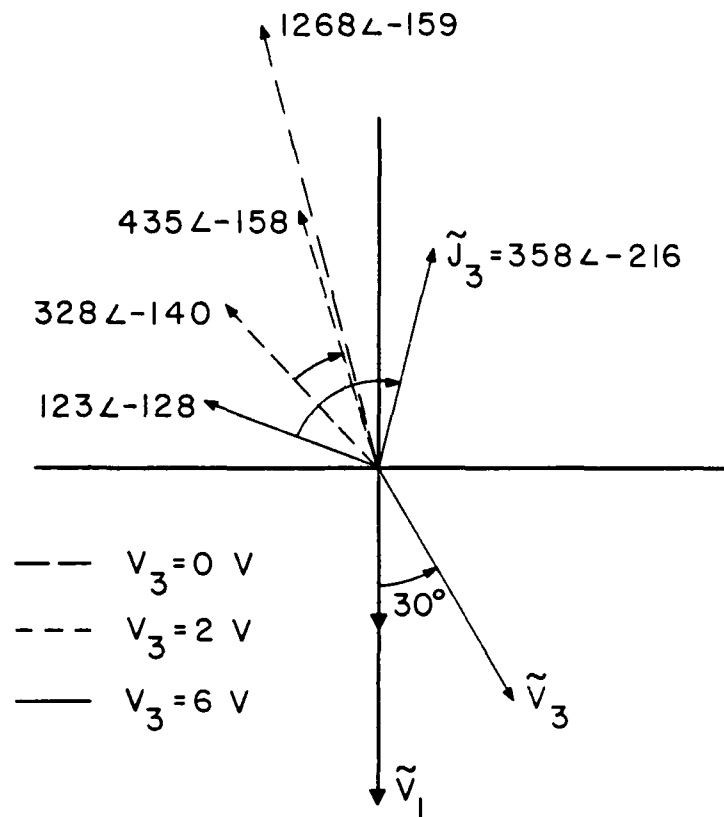
FIG. 2.27 A PHASOR DIAGRAM FOR THE THIRD-HARMONIC CURRENT

PHASOR OF THE GaAs READ DIODE AT DIFFERENT

CONDITIONS.
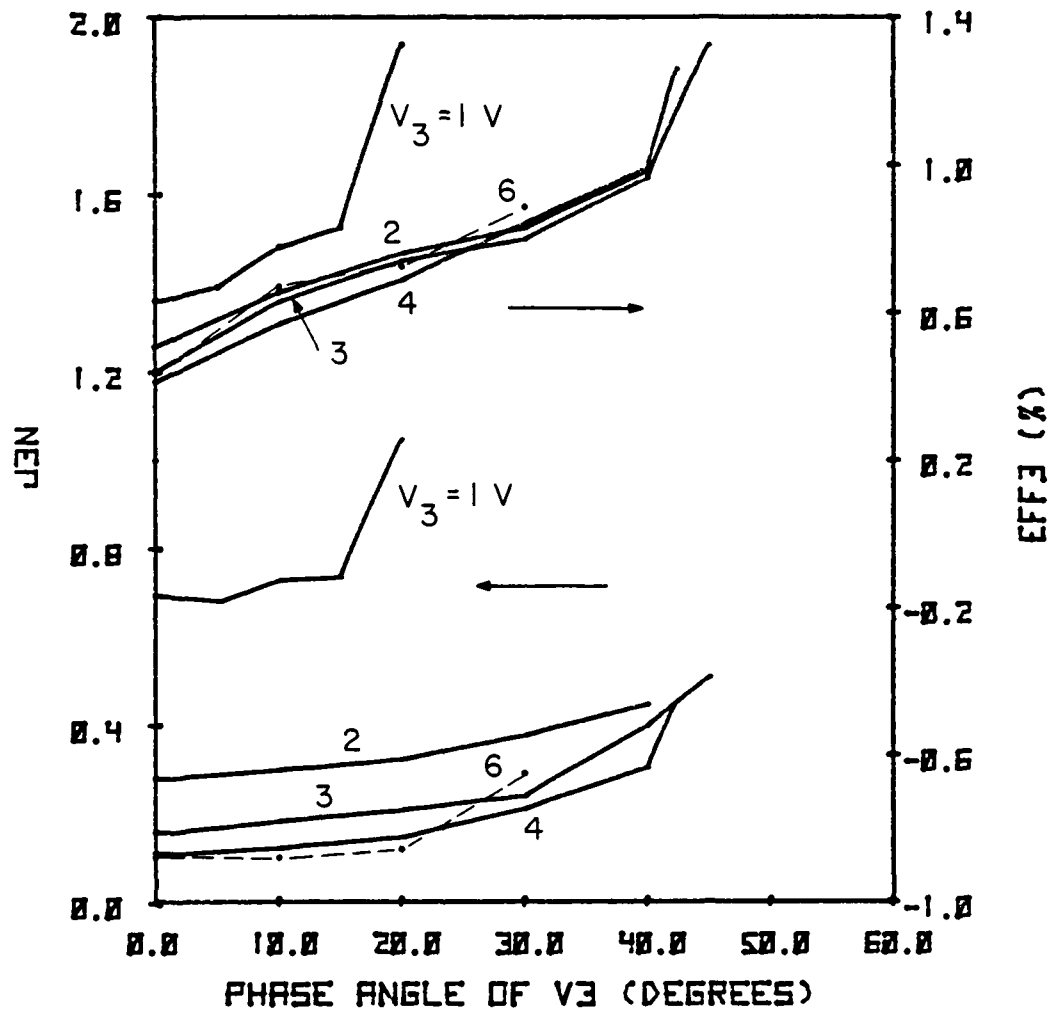
FIG. 2.28   Eff$_3$ AND J$_{3N}$ VS. θ_{3V} AT V$_1$ = 32.6 V FOR THE
GaAs READ DIODE.

voltage negative peak value changes rapidly with θ_{3V}. As a result
of the property of J_{3N}, Eff_3 decreases with V_3 first and increases
when V_3 is high. Also, Eff_3 for a fixed V_3 is an increasing function
of θ_{3V}.

As long as V_1 is high enough to induce depletion-layer modula-
tion, the behavior of J_{3N} at different values of V_1 is almost the same
except for a minor difference in the magnitude attributed to the
dependence of depletion-layer modulation on the terminal voltage. It
is expected that for the same V_3 and θ_{3V}, J_{3N} is an increasing
function of V_1. Therefore, Eff_3 increases with V_1, until active mode
operation cannot be maintained.

The maximum attainable Eff_3 at each V_3, denoted as Eff_{3max}, is
plotted in Fig. 2.29 with V_1 as a parameter. For $V_1 = 31$ V, Eff_{3max}
monotonically increases with V_3 because depletion-layer modulation is
not important. For $V_1 > 32$ V, Eff_{3max} peaks between $V_3 = 2$ and 4 V,
but drops as V_3 gets higher. This is obviously the consequence of a
rapid change of θ_{3I} with V_3. An interesting aspect in this figure
is the fall off of Eff_{3max} around $V_3 = 2$ V for $V_1 = 32.4$ and 32.6 V.
This can be understood from Fig. 2.28 in which J_{3N} decreases signifi-
cantly around $V_3 = 2$ V.

Overall, the optimum third-harmonic efficiency for this diode
is 1.67 percent at $V_1 = 33$ V, $V_3 = 4$ V, and $\theta_{3V} = 30$ degrees.

It was shown previously that the Si hybrid diode in single-
frequency operation exhibits a slow rise in J_{3N} with V_1, compared
with that of the GaAs Read diode. This results in a great difference
in third-harmonic performance between these two diodes. The difference
can be understood by comparing their induced current waveforms.
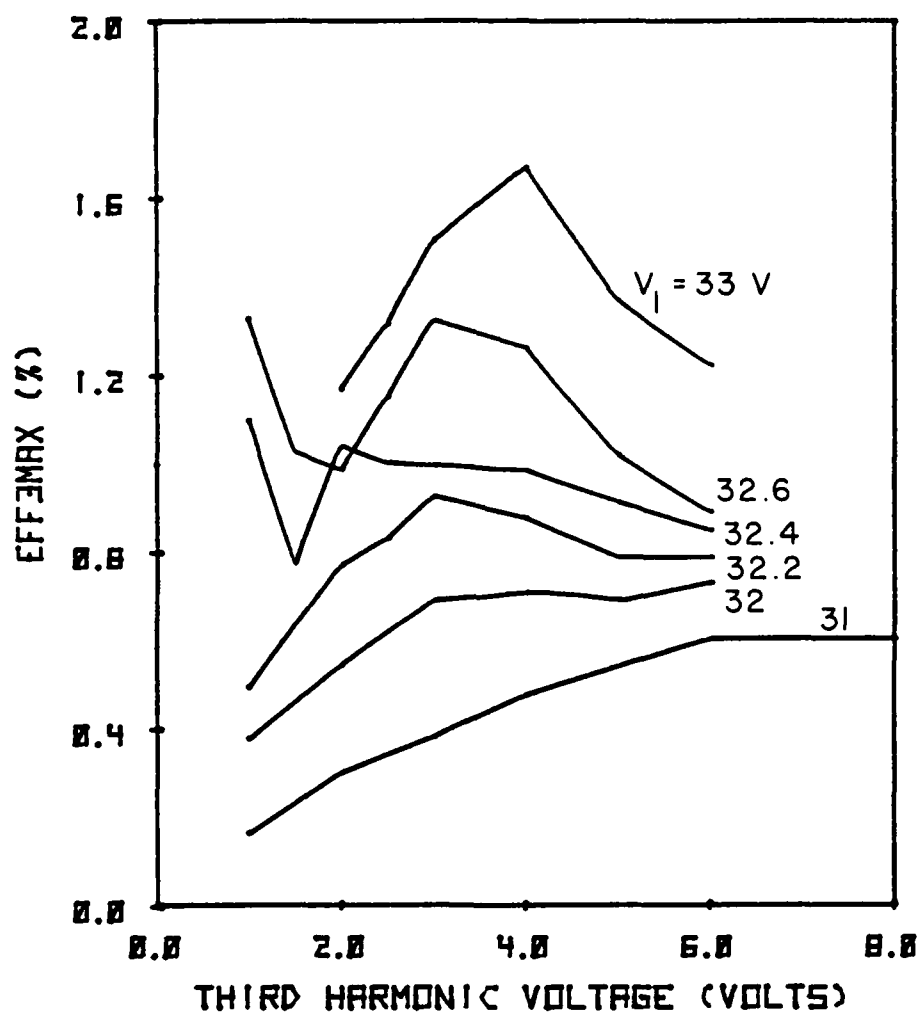
FIG. 2.29 MAXIMUM Eff$_3$ VS. THIRD-HARMONIC VOLTAGE AT
         DIFFERENT FUNDAMENTAL VOLTAGE AMPLITUDES
         FOR A GaAs READ DIODE.

Figure 2.30 shows the terminal voltage and current waveforms of
this Si diode at $V_1 = 50$ V.

At $V_3 = 2$ V, the induced current for $\theta_{3V} = 0$ degrees, shown in
Fig. 2.30a, has a minimum value of - 0.39 kA/cm^2 at $\omega t = 266.6$ degrees
in the cycle, compared with the value of - 1.21 kA/cm^2 at $\omega t = 270$
degrees in the single-frequency case. The change in the induced
current waveform gives rise to a reduction in J_3 from 1138 A/cm^2 to
971 A/cm^2 and a slight increase in θ_{3I} from - 158.8 to -158.1 degrees.
Figure 2.30a shows the induced current waveform for $\theta_{3V} = 30$ degrees.
The induced current minimum is now - 0.89 kA/cm^2 at $\omega t = 273.6$ degrees.
This corresponds to an increase of J_3 to 1028.8 A/cm^2 and a decrease
of θ_{3I} to - 165.7 degrees. The change in the injected current is too
small to affect J_3.

At $V_3 = 6$ V, the induced current for $\theta_{3V} = 0$ degrees, shown in
Fig. 2.31b, suffers a great change compared to Fig. 2.30a for $V_3 =$
2 V. The variation in the induced current waveform around $\omega t = 270$
degrees is apparently due to two minima in the voltage waveform. At
this condition, J_3 reduces to 585 A/cm^2 and θ_{3I} becomes - 159.8
degrees. For $\theta_{3V} = 30$ degrees, as shown in Fig. 2.31b, the induced
current dips at $\omega t = 288$ degrees in the cycle with a minimum value of
- 1.96 kA/cm^2. However, the dip shape becomes wider than that in the
single-frequency case. As a result, J_3 is only 922 A/cm^2 but θ_{3I}
decreases to - 194 degrees. It is noted that the third-harmonic
current phasor rotates clockwise in the phasor plane as θ_{3V} varies.

In comparison with the GaAs Read diode, the Si diode exhibits
moderate dependence of J_3 and θ_{3V} on the third-harmonic voltage.
Figure 2.32 plots J_{3N} and Eff$_3$ vs. θ_{3V} for several values of V_1.

SI HYBRID

JDC=1600   T=500

V=50 ,0.2   Q=0,0.0

FREQUENCY =   23.00 GHZ

SI HYBRID

JDC=1600   T=500

V=50 ,0.2   Q=0,0.30

FREQUENCY =   23.00 GHZ

(a)

(b)
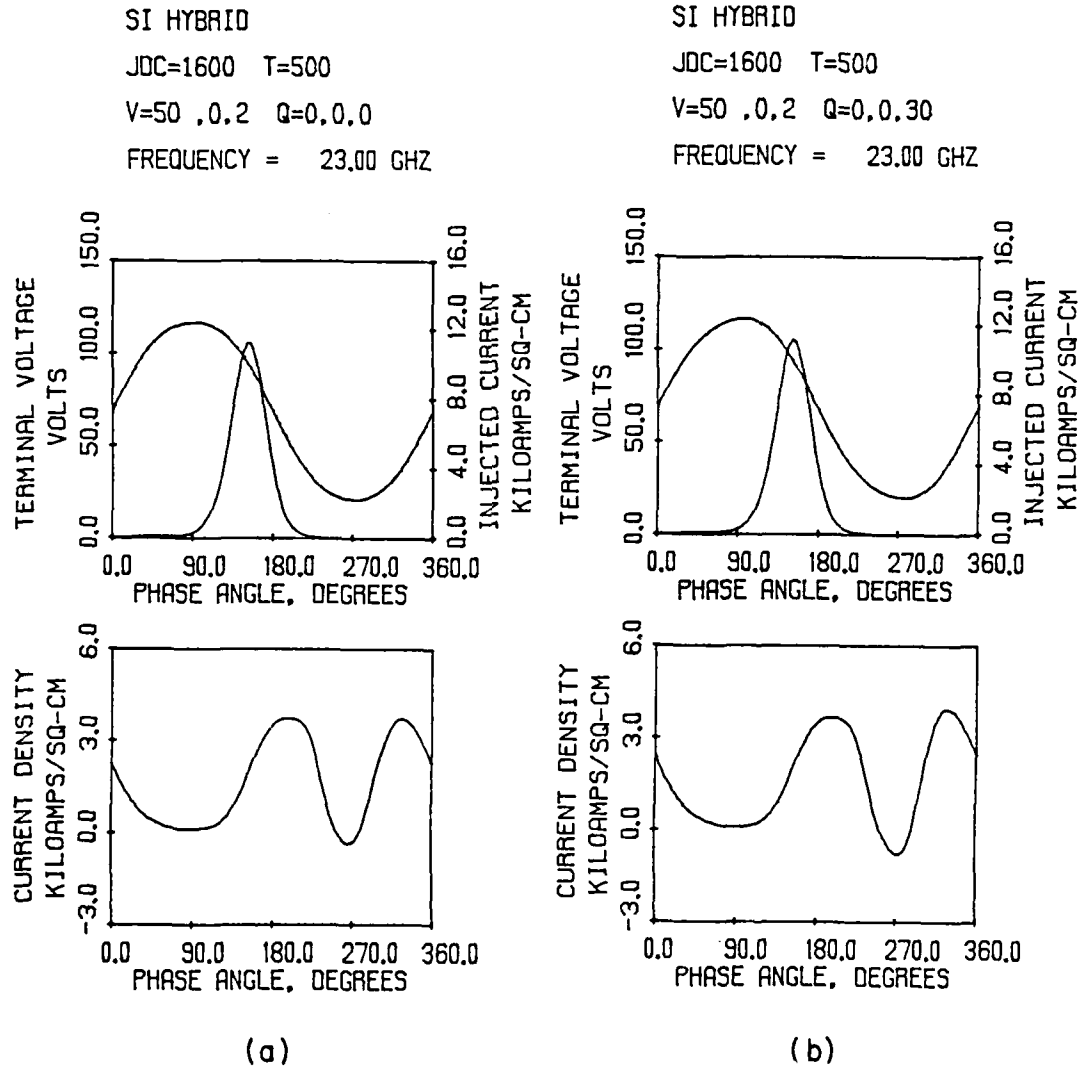
FIG. 2.30   LARGE-SIGNAL SOLUTIONS FOR A Si HYBRID DIODE AT

(a) V_1 = 50 V, V_3 = 2 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 50 V, V_3 = 2 V AND θ_{3V} = 30 DEGREES.

SI HYBRID

JDC=1600   T=500

V=50 ,0.6   Q=0.0.0

FREQUENCY =   23.00 GHZ

SI HYBRID

JDC=1600   T=500

V=50 ,0.6   Q=0.0.30

FREQUENCY =   23.00 GHZ

(a)

(b)
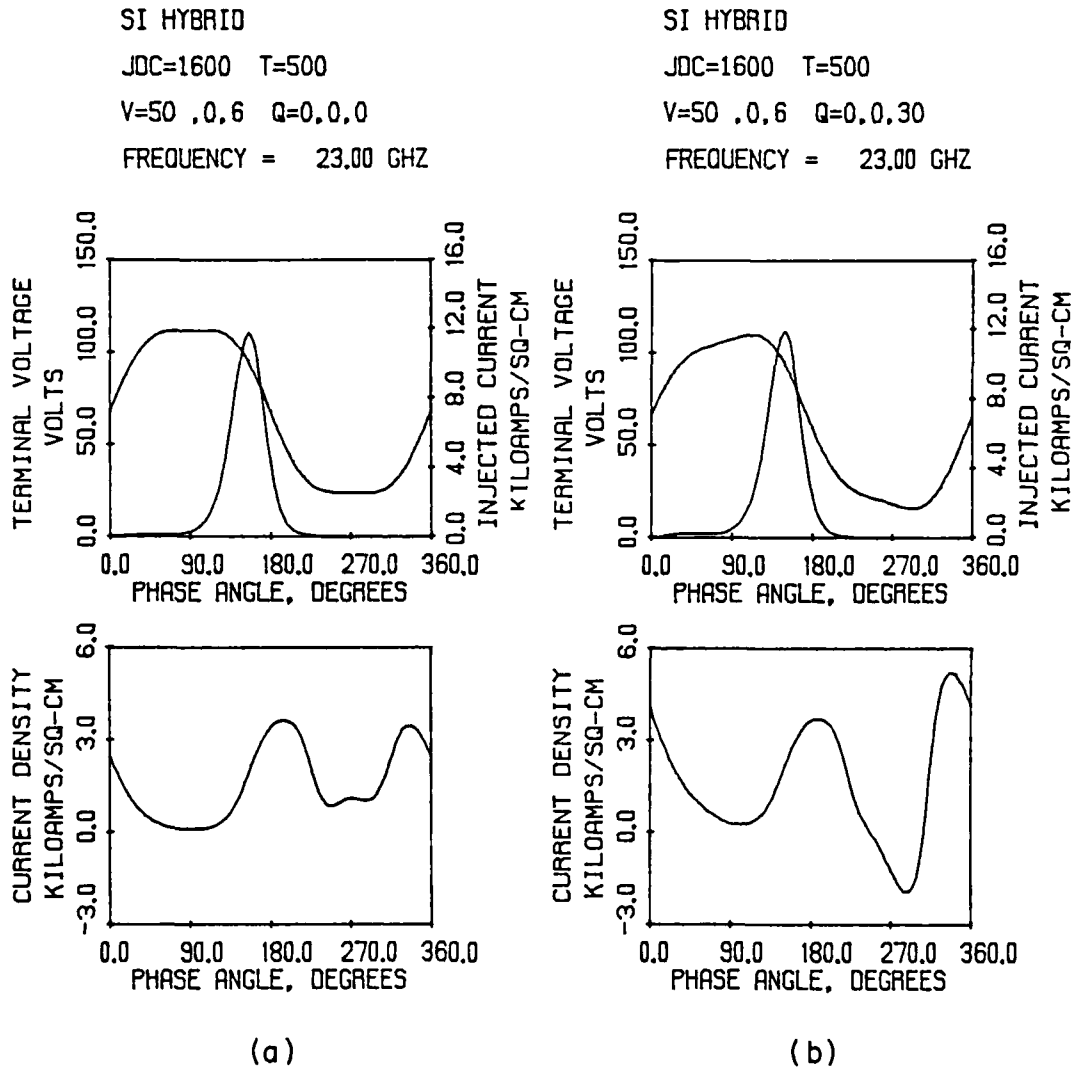
FIG. 2.31   LARGE-SIGNAL SOLUTIONS FOR A Si HYBRID DIODE AT

(a) V_1 = 50 V, V_3 = 6 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 50 V, V_3 = 6 V AND θ_{3V} = 30 DEGREES.
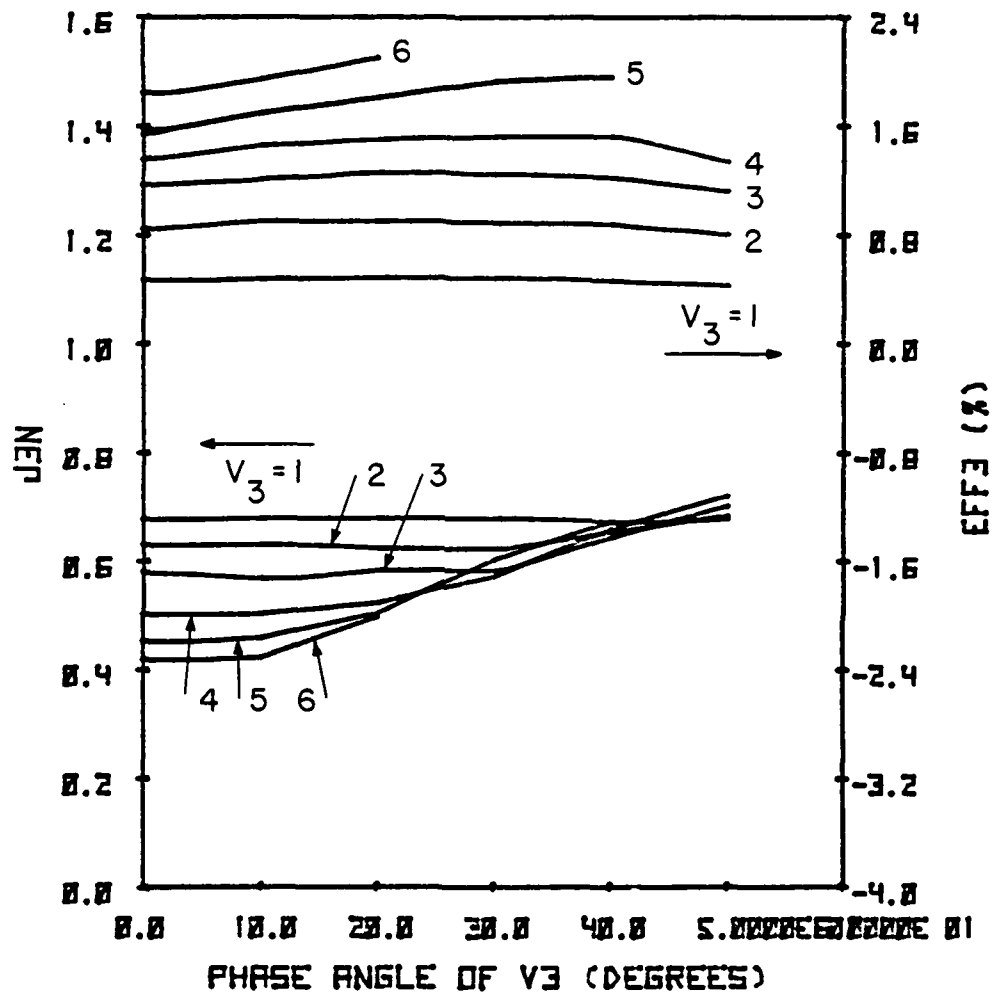
FIG. 2.32 J_{3N} AND Eff_3 VS. θ_{3V} AT V_1 = 50 V FOR A SI HYBRID DIODE
IN TWO-FREQUENCY OPERATION.

The slow reduction in J_{3N} with increasing V_3 can be observed. Because of this slow reduction, Eff_3 increases gradually with V_3 until active mode operation is no longer maintained. The behavior of Eff_3 of this diode differs from that in the GaAs Read diode. Hence, higher Eff_3 can be achieved in this diode.

Figure 2.33 plots Eff_{3max} vs. V_3 for several values of V_1. Eff_{3max} is observed to increase with V_1 until Eff_1 becomes negative. It is found from simulation that when V_1 exceeds 52 V, active mode operation is impossible to achieve due to the fact that the dip in the induced current waveform is too wide to make Eff_1 positive. This greatly restricts the third-harmonic power generation capability of this diode. Therefore, it is unlikely that this diode will be operated at high V_1 to generate harmonic power. The optimum third-harmonic efficiency found from the simulation is 2.1 percent at V_1 = 50 V, V_3 = 6 V, and θ_{3V} = 20 degrees.

The Si uniform diode can achieve an optimum third-harmonic efficiency of 3.1 percent which occurs at V_1 = 65.4 V, V_3 = 7 V and θ_{3V} = 15 degrees. This diode shows much better harmonic performance than the previous two diodes. In single-frequency operation, this diode, owing to its high doping concentration, can produce high third-harmonic current which varies slowly with terminal voltage level. With this property, J_3 in multifrequency operation is expected to be less influenced by the presence of V_3 in the terminal voltage. The induced current and voltage waveforms plotted in Figs. 2.34 and 2.35 are used to examine the influence of V_3 on J_3 for V_1 = 64 V.
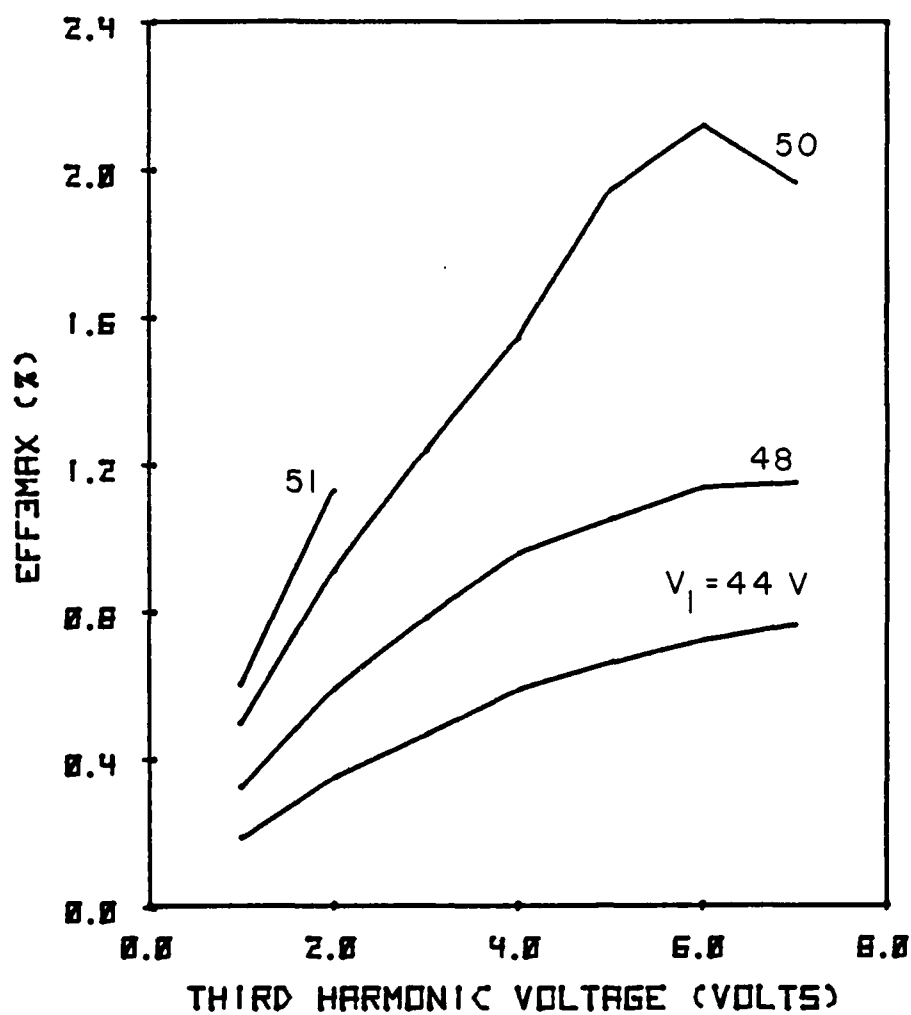
FIG. 2.33 MAXIMUM Eff₃ VS. THIRD-HARMONIC VOLTAGE AT DIFFERENT FUNDAMENTAL VOLTAGE AMPLITUDES FOR A Si HYBRID DIODE.

SI UNIFORM

  JDC=2400 T=500

  V=64 ,0.3 Q=0,0,0

  FREQUENCY = 23.00 GHZ

SI UNIFORM

  JDC=2400 T=500

 V=64 ,0.3 Q=0,0,30

  FREQUENCY = 23.00 GHZ

(a)   (b)
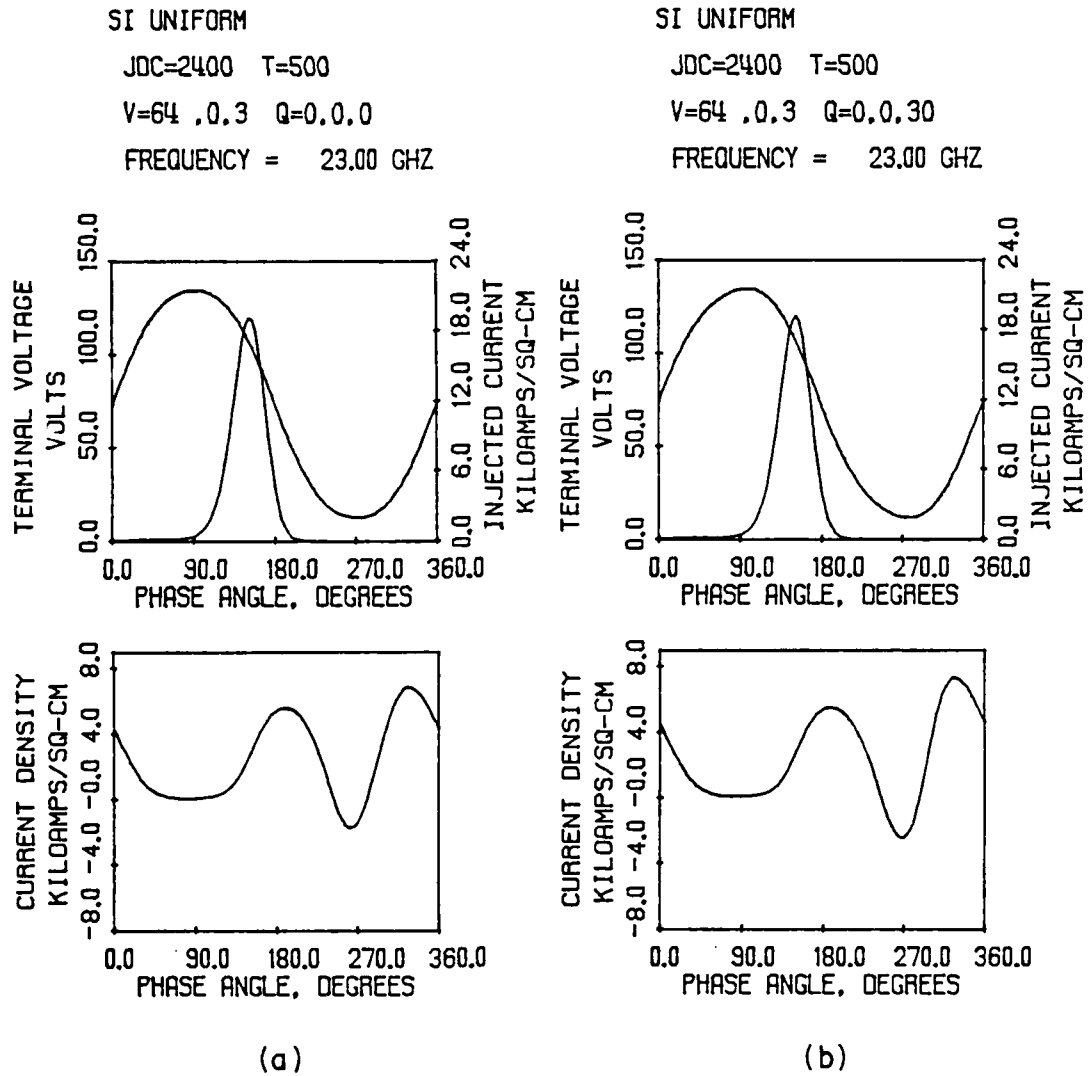
FIG. 2.34 LARGE-SIGNAL SOLUTIONS FOR A Si UNIFORM DIODE AT

(a) V_1 = 64 V, V_3 = 3 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 64 V, V_3 = 3 V AND θ_{3V} = 30 DEGREES.

SI UNIFORM
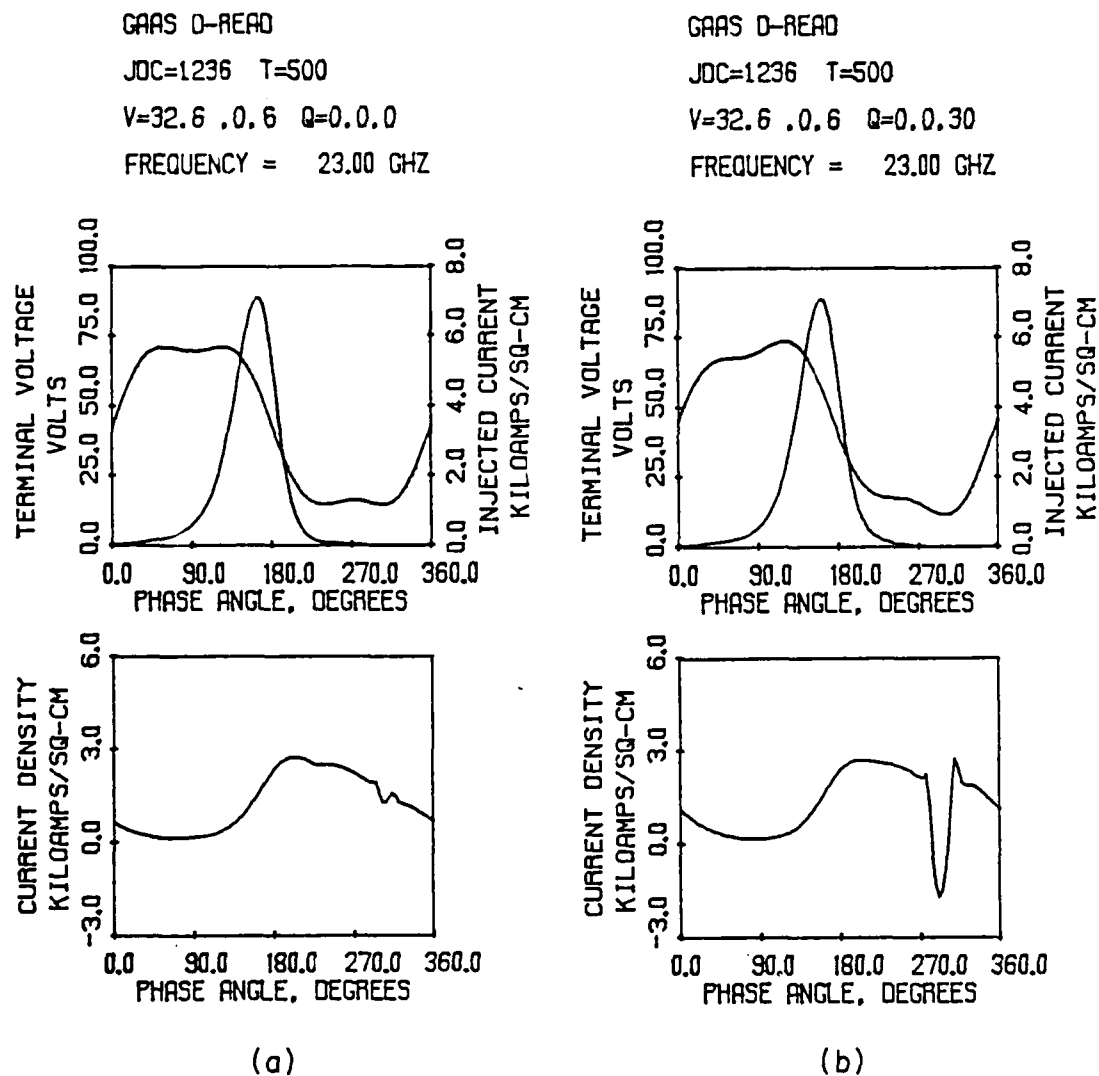
JDC=2400 T=500

V=64 .0.9 Q=0.0.0

FREQUENCY =   23.00 GHZ

SI UNIFORM

JDC=2400 T=500

V=64 .0.9 Q=0.0.30

FREQUENCY =   23.00 GHZ

(a)

(b)

FIG. 2.35 LARGE-SIGNAL SOLUTIONS FOR A Si UNIFORM DIODE AT

(a) V_1 = 64 V, V_3 = 9 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 64 V, V_3 = 9 V AND θ_{3V} = 30 DEGREES.

At $V_3 = 3$ V, as shown in Fig. 2.34, the terminal RF voltage for $\theta_{3V} = 0$ degrees has a minimum value of 61 V and the corresponding induced current has a minimum value of $- 1.78$ kA/cm^2, compared with the value of $- 4.01$ kA/cm^2 in the single-frequency case. Consequently, J_3 decreases from 2231 to 1717.9 A/cm^2 and θ_{3I} is now $- 154.6$ degrees. As θ_{3V} increases to 30 degrees, the current minimum value becomes $- 2.43$ kA/cm^2 and the dip position shifts from 262.8 degrees for $\theta_{3V} = 0$ degrees to 270 degrees. This leads to an increase of J_3 to 1835.9 A/cm^2 and a decrease of θ_{3I} to $- 163.3$ degrees. No significant change in the injected current waveform was observed.

At $V_3 = 9$ V, as shown in Fig. 2.35a, the induced current for $\theta_{3V} = 0$ degrees has two minima with different values (positive). J_3 drops to 694.8 A/cm^2 and θ_{3I} becomes $- 175$ degrees. For $\theta_{3V} = 30$ degrees, the induced current dips at $\omega t = 288$ degrees with a minimum value of $- 3.5$ kA/cm^2. The corresponding J_3 increases to 1517.2 A/cm^2 and θ_{3I} decreases to $- 204$ degrees. It is apparent from Fig. 2.35b that the dip becomes wider than that in the single-frequency case. Hence J_3 at this condition is still less than that in the single-frequency case. The phase difference $\theta_{3V} - \theta_{3I}$ is now $- 126$ degrees and the corresponding $\cos (\theta_{3V} - \theta_{3I})$ is 0.59, which is far less than unity. Therefore, Eff$_3$ will decrease beyond $\theta_{3V} = 30$ degrees.

J_{3N} and Eff$_3$ vs. θ_{3V} with V_3 as a parameter are plotted in Fig. 2.36 for $V_1 = 64$ V. Comparison at the same V_3 shows that this diode can have a higher J_{3N} than the Si hybrid diode at $V_1 = 50$ V. As a result, this diode can achieve higher Eff$_3$. From the figure, Eff$_3$ for a given V_3 always reaches a maximum value around $\theta_{3V} = 30$ degrees. This is because θ_{3I} is always between $- 154$ and $- 180$
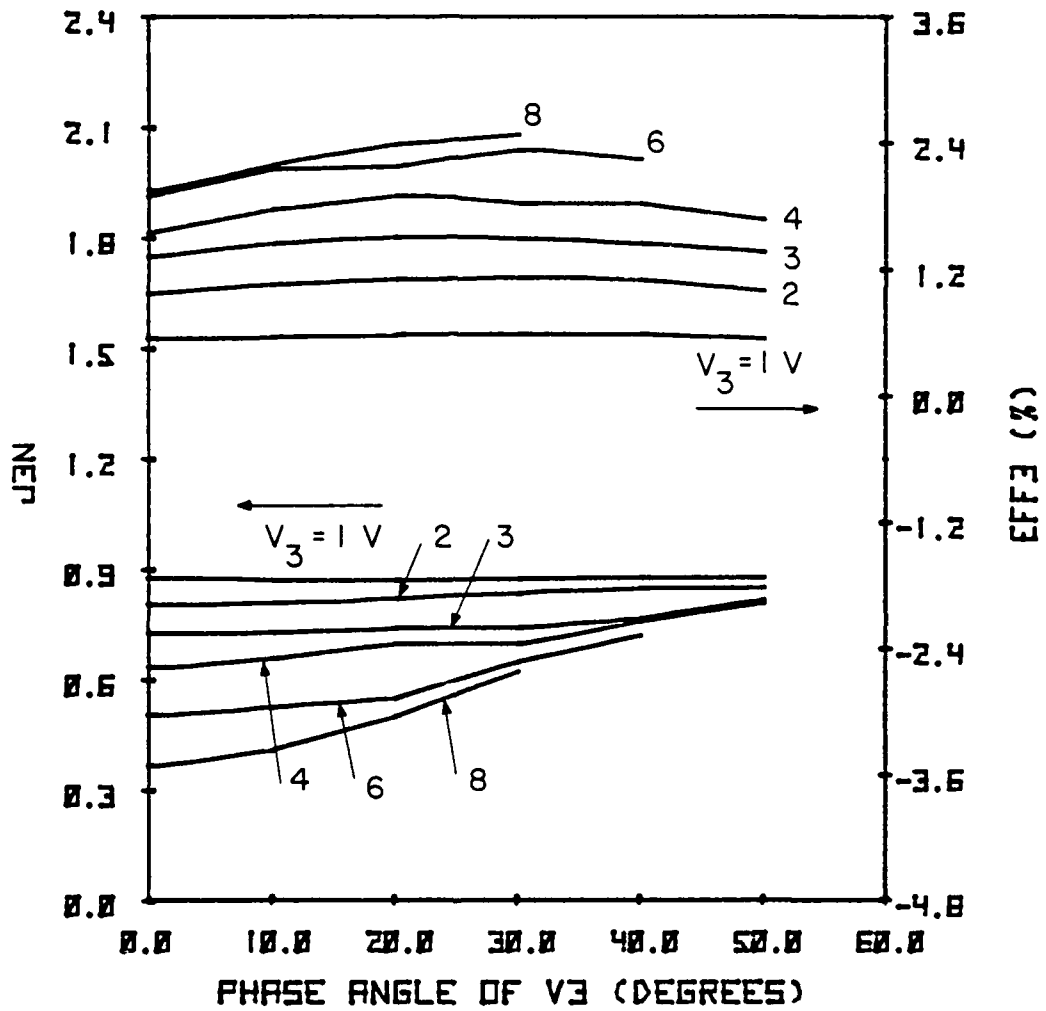
FIG. 2.36 J_{3N} AND Eff_3 VS. θ_{3V} AT $V_1 = 64$ V FOR A Si UNIFORM DIODE IN TWO-FREQUENCY OPERATION.

degrees and J_{3N} does not show a great dependence on θ_{3V}. However, the dependence of θ_{3I} on V_3 and θ_{3V} gives rise to the small change in Eff_3 between $V_1 = 6$ and 8 V.

Eff_{3max} as a function of V_3 is plotted in Fig. 2.37 with V_1 as a parameter. Eff_{3max} shows a sign of saturation around $V_3 = 7$ V for $V_1 \geq 62$ V. Furthermore, for $V_1 = 54$ V, Eff_{3max} is low and increases very slowly with V_3. Therefore, in terms of third-harmonic efficiency, it seems to be unfavorable to operate this diode at either low V_1 or high V_3 for harmonic power generation.

The GaAs uniform diode can achieve an optimum third-harmonic efficiency of 4.16 percent at $V_1 = 37.4$ V, $V_3 = 4.5$ V, and $\theta_{3V} = 30$ degrees. From the results of single-frequency operation, this diode can have a higher J_{3N} than the other diodes and also have a small phase delay in the third-harmonic current. As a result, this diode can achieve better third-harmonic performance. A detailed investigation about the effects of third-harmonic voltage on device performance is given in the following.

Figures 2.38 and 2.39 plot the induced current and terminal voltage waveforms for $V_1 = 37$ V. At $V_3 = 2$ V the induced current waveform for $\theta_{3V} = 0$ degrees, shown in Fig. 2.38a, has a minimum value of -2.59 kA/cm^2 at $\omega t = 255.6$ degrees in the cycle compared with the value of -5.92 kA/cm^2 for the single-frequency case. The corresponding J_3 decreases from 3320.4 A/cm^2 to 2524.8 A/cm^2 and θ_{3I} has a value of -127.1 degrees, which is the same as that in the single-frequency case. When θ_{3V} becomes 30 degrees, the induced current has a minimum value of -3.26 kA/cm^2 at $\omega t = 262.8$ degrees. Consequently, J_3 increases to 2708.5 A/cm^2 and θ_{3I} decreases to -138.2
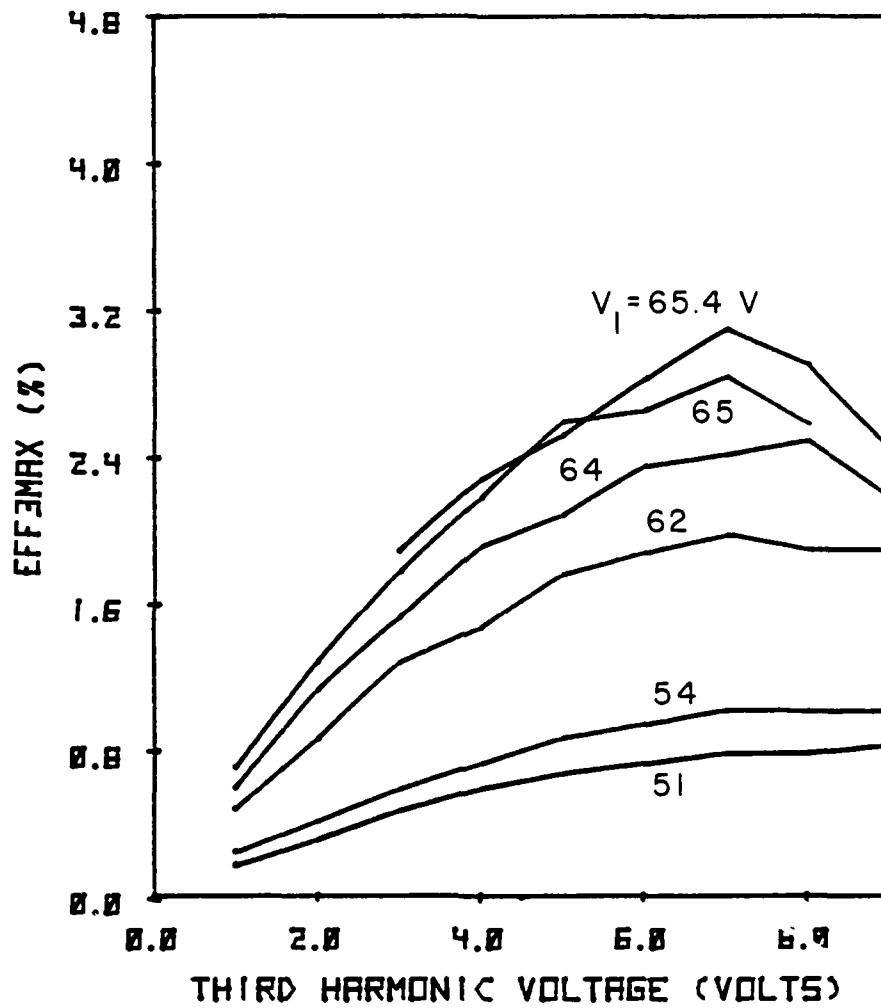
FIG. 2.37 MAXIMUM Eff$_3$ VS. THIRD-HARMONIC VOLTAGE AT DIFFERENT
FUNDAMENTAL VOLTAGE AMPLITUDES FOR A Si UNIFORM DIODE.

-116-

GAAS UNIFORM

JDC=3200 T=500

V=37 ,0.2 Q=0,0,0

FREQUENCY =   23.00 GHZ

GAAS UNIFORM

JDC=3200 T=500

V=37 ,0.2 Q=0,0,30

FREQUENCY =   23.00 GHZ

(a)

(b)
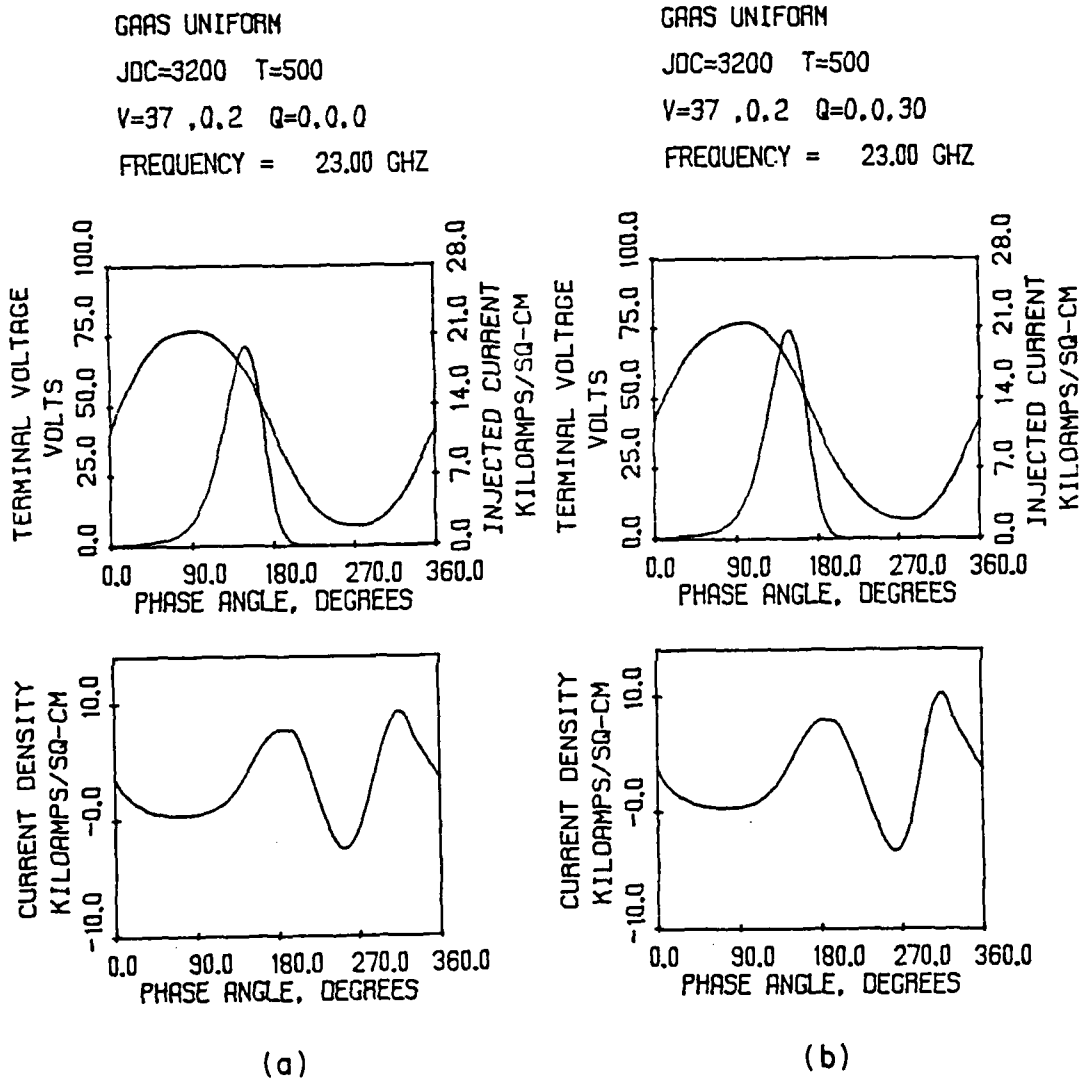
FIG. 2.38 LARGE-SIGNAL SOLUTION FOR A GaAs UNIFORM DIODE AT

(a) V_1 = 37 V, V_3 = 2 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 37 V, V_3 = 2 V AND θ_{3V} = 30 DEGREES.

GAAS UNIFORM
JDC=3200 T=500
V=37 ,0.6 Q=0,0,0
FREQUENCY = 23.00 GHZ

GAAS UNIFORM
JDC=3200 T=500
V=37 ,0.6 Q=0,0,30
FREQUENCY = 23.00 GHZ
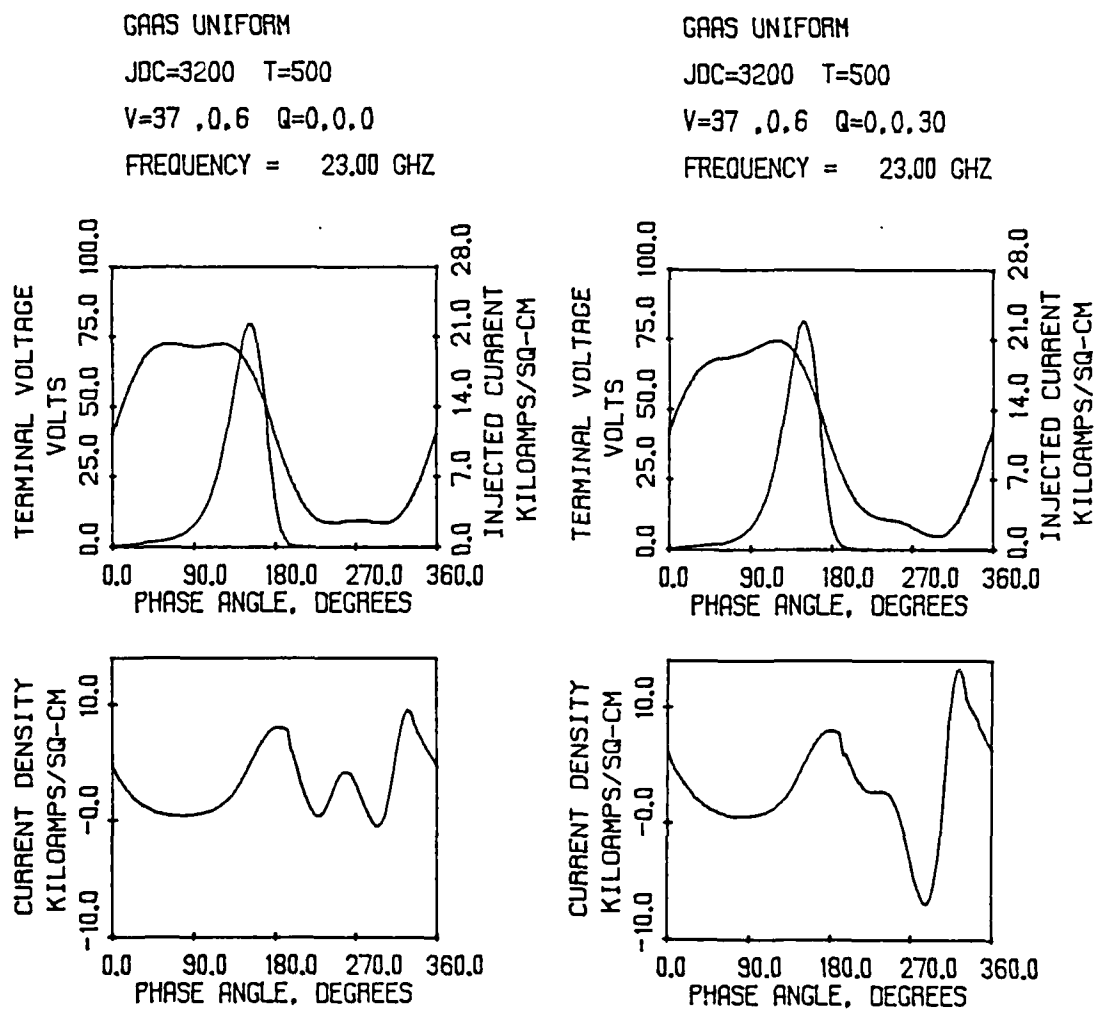
(a) (b)

FIG. 2.39 LARGE-SIGNAL SOLUTIONS FOR A GaAs UNIFORM DIODE AT

(a) V_1 = 37 V, V_3 = 6 V AND θ_{3V} = 0 DEGREES AND

(b) V_1 = 37 V, V_3 = 6 V AND θ_3 30 DEGREES.

degrees. At $V_3 = 6$ V, as shown in Fig. 2.39a for $\theta_{3V} = 0$ degrees, the terminal voltage minima have a profound effect on the induced current waveform. At this condition, J_3 is now 640.1 A/cm^2 and θ_{3I} is - 148.2 degrees. As θ_{3V} becomes 30 degrees, the induced current minimum shifts to 288 degrees and has a value of - 7 kA/cm^2. The dip in the current is not as sharp as that in the single-frequency case because of the variation in slope of the terminal voltage around $\omega t = 270$ degrees. Hence, J_3 will not be as high as in the single-frequency case. It is found that J_3 is only 2254 A/cm^2 and θ_{3I} is - 190 degrees.

In general, the magnitude of θ_{3I} in this diode is always less than that in the Si uniform diode. As indicated previously, the difference in θ_{3I} between these two diodes arises from the fact that in the GaAs uniform diode, the induced current at high RF voltages tends to dip before the voltage goes to a minimum. Consequently, for fixed V_1 and V_3, Eff$_3$ in the GaAs uniform diode reaches its maximum around $\theta_{3V} = 40$ degrees instead of 30 degrees as in the Si uniform diode. Since it is known that depletion-layer modulation will be enhanced with increasing θ_{3V}, the GaAs uniform diode can achieve higher J_{3N} at the maximum Eff$_3$ point than the Si diode. It can be concluded that the GaAs uniform diode can have higher third-harmonic efficiency than the other diode.

The normalized third-harmonic current and third-harmonic efficiency at $V_1 = 37$ V are plotted in Fig. 2.40 as functions of θ_{3V}. It is seen that J_{3N} has a higher decreasing rate with respect to V_3 than that in the Si uniform diode. This is because the GaAs diode has a shorter device length. The high decreasing rate in
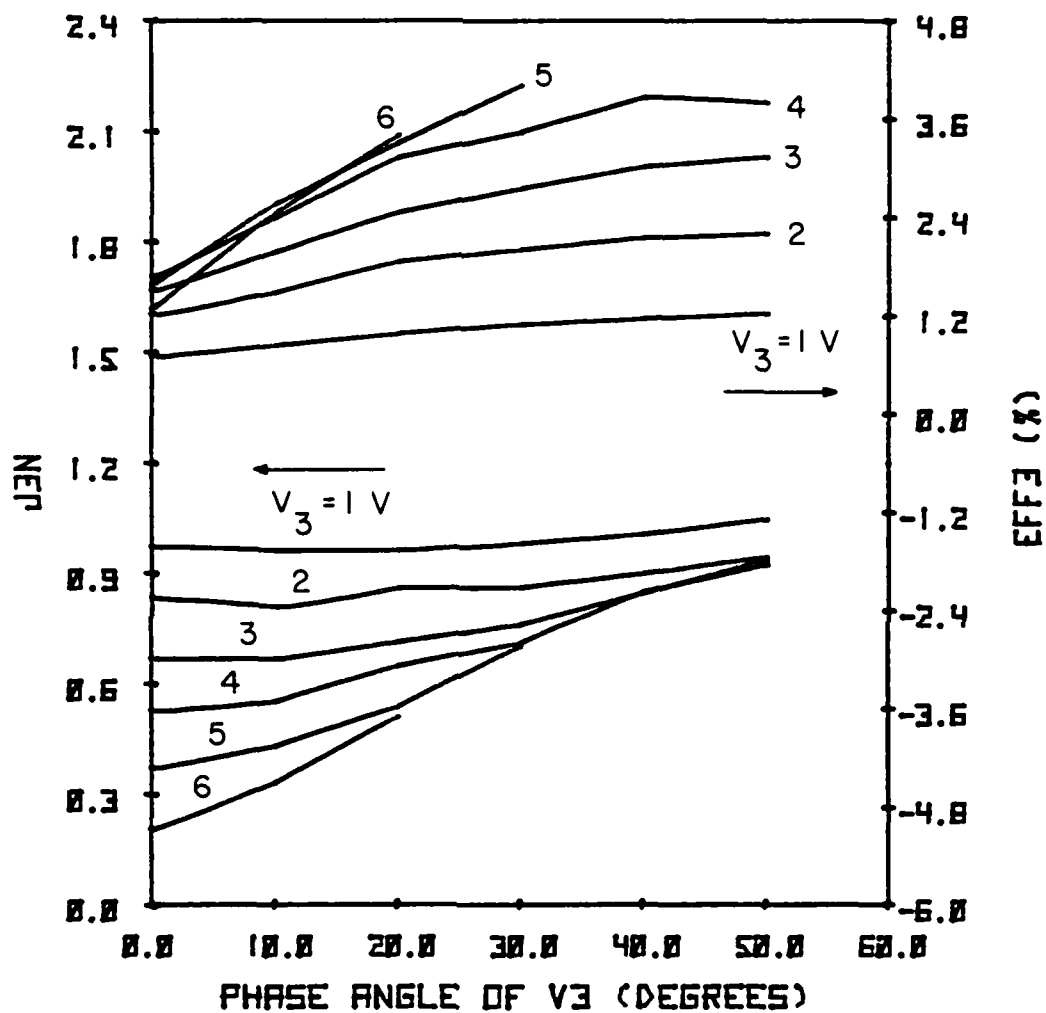
FIG. 2.40 J_{3N} AND Eff_3 VS. θ_{3V} AT $V_1 = 37$ V FOR A GaAs
UNIFORM DIODE.

J_{3N} is responsible for saturation in Eff_3 for $V_3 > 5$ V. It is also understandable that for a fixed V_3 the GaAs uniform diode has a higher increasing rate in J_{3N} with respect to θ_{3V} than other diodes.

Figure 2.41 is a plot of Eff_{3max} vs. V_3 for different values of V_1. One interesting aspect in this plot is that the GaAs uniform diode does not show a higher Eff_{3max} at $V_3 = 38$ V than at $V_1 = 37.4$ V. This is primarily because at V_1 as high as 38 V, active mode operation cannot be maintained for θ_{3V} deviating from zero degrees. As before, for a fixed V_1, Eff_{3max} saturates for V_3 around 6 V. This limits the capability of this diode for third-harmonic power generation.

2.3.4b Second-Harmonic Performance for the Si Uniform

Diode. The Si uniform diode is chosen to study its second-harmonic performance because it can achieve higher second-harmonic current generation in single-frequency operation than other diodes investigated. In this study the terminal RF voltage is given by

$$V_t = V_1 \sin (\omega t) + V_2 \sin (2\omega t + \theta_{2V}) \qquad (2.47)$$

and the second-harmonic output power and efficiency are calculated by

$$P_2 = -\frac{1}{2} V_2 J_2 \cos (\theta_{2I} - \theta_{2V}) \qquad (2.48)$$

and

$$Eff_2 = -\frac{1}{2} V_{2N} J_{2N} \cos (\theta_{2I} - \theta_{2V}) \ , \qquad (2.49)$$

where θ_{2V} is the phase angle of the second-harmonic voltage relative to the fundamental voltage, $J_{2N} = J_2/I_{dc}$, and $V_{2N} = V_2/V_{dc}$. In order to achieve high second-harmonic power generation in active mode operation, it is needed to keep V_1 as high as possible to induce
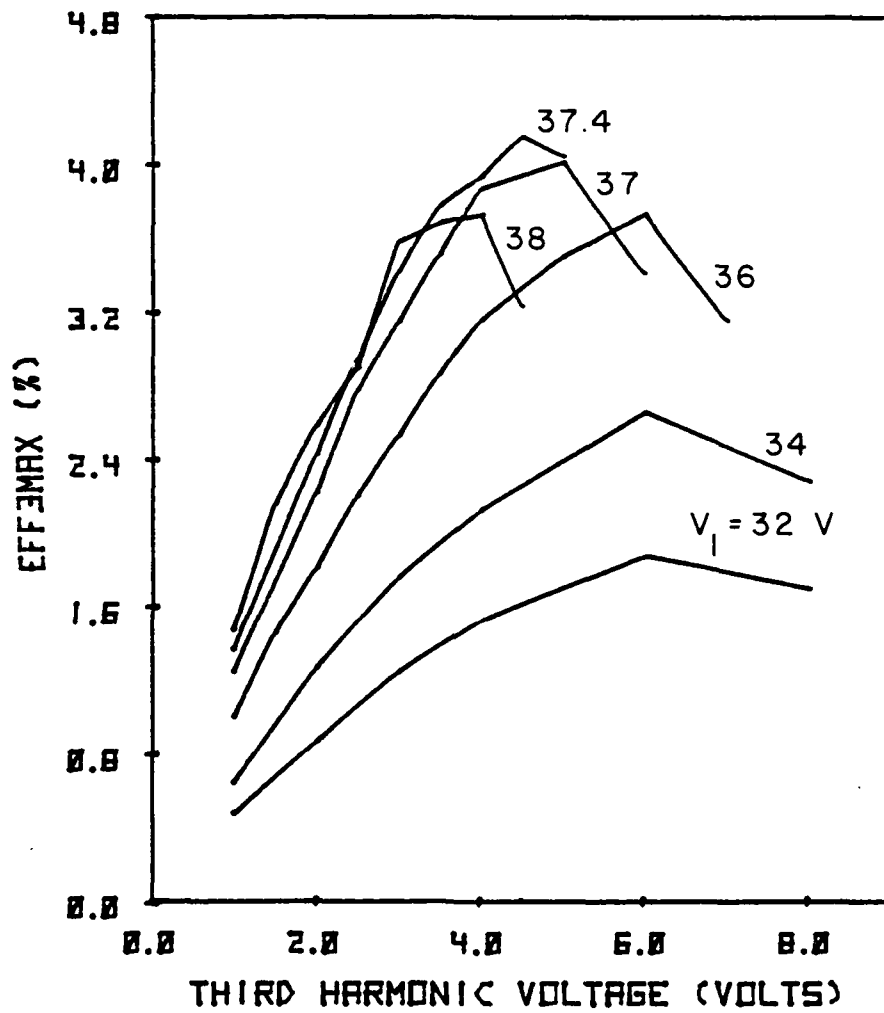
FIG. 2.41 MAXIMUM Eff$_3$ VS. THIRD-HARMONIC VOLTAGE AT DIFFERENT
FUNDAMENTAL VOLTAGE MAGNITUDES FOR A GaAs UNIFORM
DIODE.

depletion-layer modulation and to choose an appropriate V_2 and θ_{2V} not only to shift the induced current minimum away from the fundamental voltage minimum but also to yield $\theta_{2I} - \theta_{2V} = 180$ degrees. From the simulation results presented in Table 2.4 it is expected that for a fixed V_1, Eff_2 can reach its maximum provided that θ_{2V} is around -70 degrees and V_2 is not too high. Therefore, it is worthwhile to examine the resulting terminal RF voltage in the presence of a small second-harmonic voltage.

Figure 2.42 plots the normalized terminal RF voltage V_{tN} ($V_{tN} = V_t/V_1$) for $V_2/V_1 = 1/5$ with $\theta_{2V} = -90$ to 0 degrees. This normalized voltage waveform has two asymmetric portions (positive and negative going). For $\theta_{2V} = -90$ degrees, the negative-going portion is almost flat, approximately $\omega t = 270$ degrees, but the positive-going portion is sharp. As θ_{2V} increases, the voltage minimum in an almost similar manner as the case shown in Fig. 2.24a shifts toward $\omega t = 270$ degrees with an increase in magnitude. Therefore, it is expected that increasing θ_{2V} will enhance depletion-layer modulation. In contrast, the voltage maximum value decreases with increasing θ_{2V}. This affects the formation of the injected current. Also, the zero-crossing point of the voltage waveform shifts to the left of $\omega t = 180$ degrees. The extent of this shift depends on the ratio of V_2/V_1. Nevertheless, the injected current waveform shifts to the left. It can be derived for $\theta_{2V} = -90$ degrees, the voltage has only a minimum provided that $V_2/V_1 \leq 1/4$. With this property, a high second-harmonic voltage can be applied to the terminal without causing two minima in the terminal voltage waveform. It was known from the
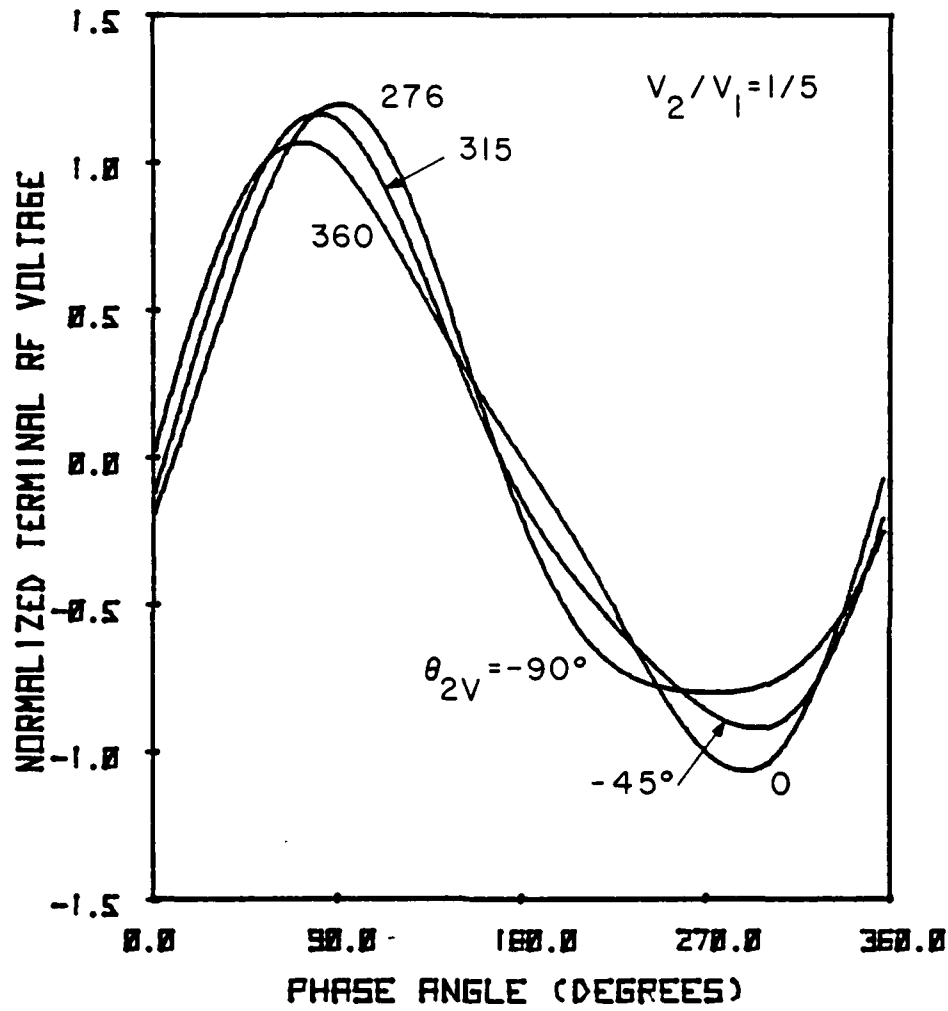
FIG. 2.42 PLOTS OF $V_t = \sin \omega t + (1/5) \sin (2\omega t + \theta_{2V})$ VS. ωt.

previous study that the appearance of two voltage minima deteriorates the dip shape and increases the phase delay of harmonic current.

The terminal voltage and current waveforms for $V_1 = 64$ V and $V_2 = 10$ V are plotted in Fig. 2.43. For $\theta_{2V} = - 90$ degrees, the terminal voltage has a minimum value of $- 54$ V at $\omega t = 270$ degrees in the cycle. The corresponding induced current has a minimum value of $- 1.5$ kA/cm^2, compared with the value of $- 4.01$ kA/cm^2 for the single-frequency case. J_2 and θ_{2I} are now 1725.4 A/cm^2 and 112 degrees, respectively, compared with 3487 A/cm^2 and 98.6 degrees for the single-frequency case. For $\theta_{2V} = - 45$ degrees, the induced current waveform shown in Fig. 2.43b has a significant dip because of the change in the terminal voltage. The induced current now has a minimum value of $- 2.05$ kA/cm^2 at $\omega t = 280.8$ degrees. Consequently, J_2 increases to 2828.3 A/cm^2 but θ_{2I} decreases to 91.4 degrees. In comparison with the third-harmonic performance of this diode at the same V_1, the second-harmonic voltage does not affect the second-harmonic current significantly. The primary reason may be due to the difference in the resulting terminal RF voltage waveform. For the third-harmonic case, the terminal RF voltage waveform has two minima for $\theta_{3V} = 0$ degrees, if $V_3 > V_1/9$. For the second-harmonic case, the voltage waveform has two minima at $\theta_{2V} = - 90$ degrees only if $V_2 > V_1/4$.

Detailed second-harmonic performance at $V_1 = 64$ V is shown in Fig. 2.44. It is seen that J_{2N} slowly decreases with increasing V_2 and is always above 0.3 in the range of V_2 indicated in the figure. As a result, Eff_2 is usually greater than Eff_3 shown in Fig. 2.36. The maximum Eff_2 achievable at $V_1 = 64$ V is 8.71 percent, compared

SI UNIFORM

JDC=2400   T=500

V=64 ,10.0   Q=0,   -90

FREQUENCY =   23.00 GHZ

SI UNIFORM

JDC=2400   T=500

V=64 ,10.0   Q=0,   -45

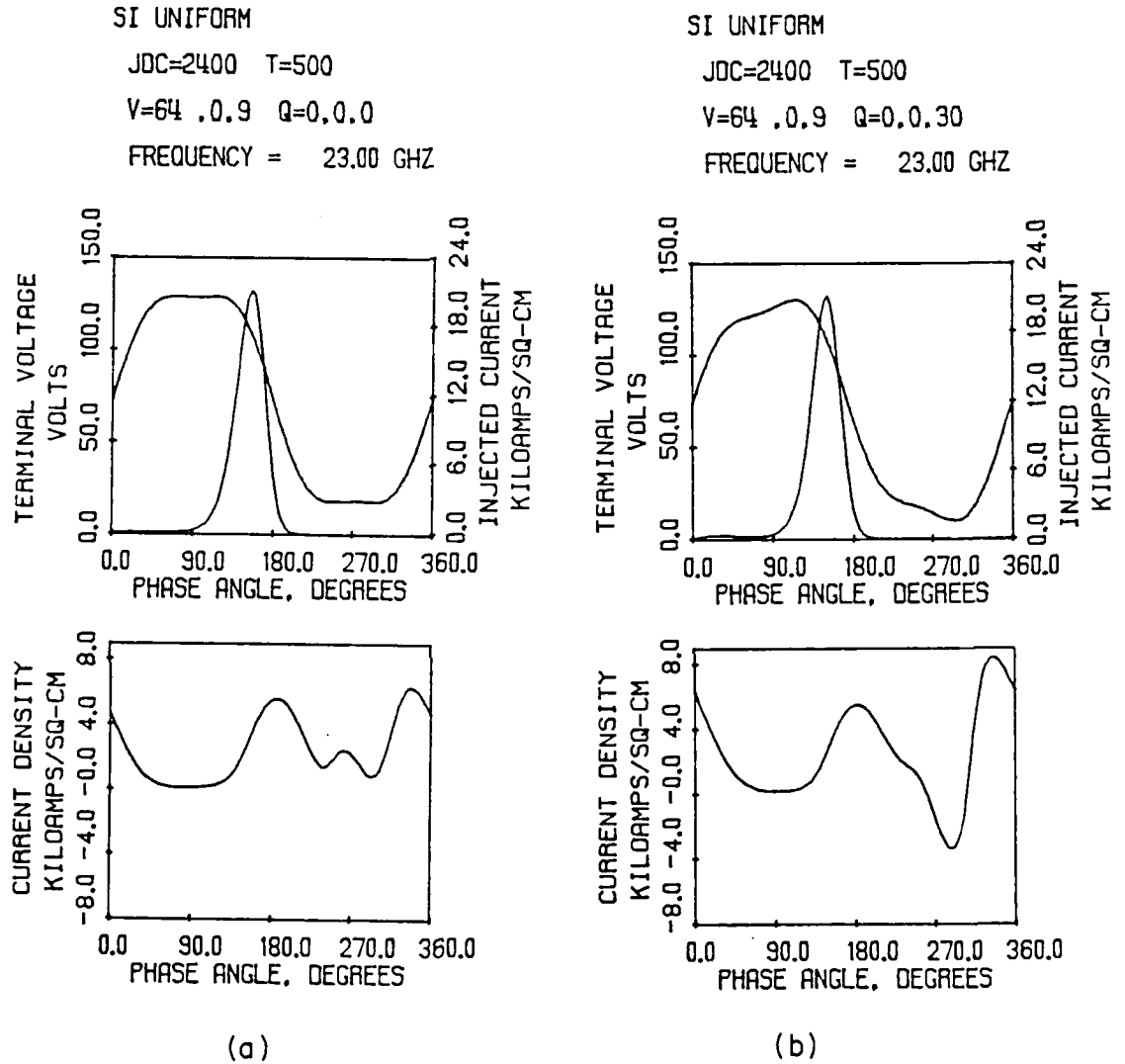FREQUENCY =   23.00 GHZ

(a)

(b)
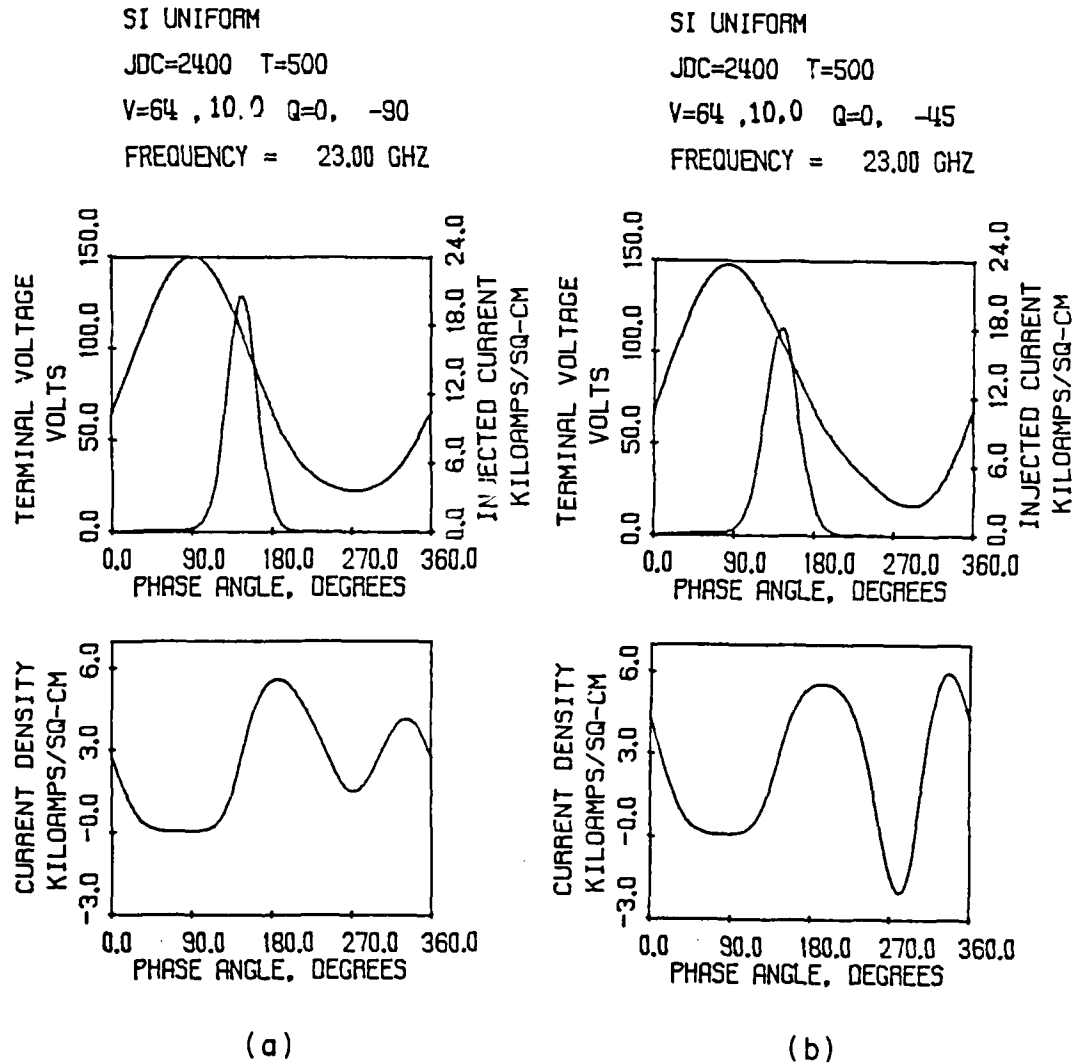
FIG. 2.43   LARGE-SIGNAL SOLUTIONS FOR A Si UNIFORM DIODE AT

(a) $V_1 = 64$ V, $V_2 = 10$ V AND $\theta_{2V} = -90$ DEGREES AND

(b) $V_1 = 64$ V, $V_2 = 10$ V AND $\theta_{2V} = -45$ DEGREES.
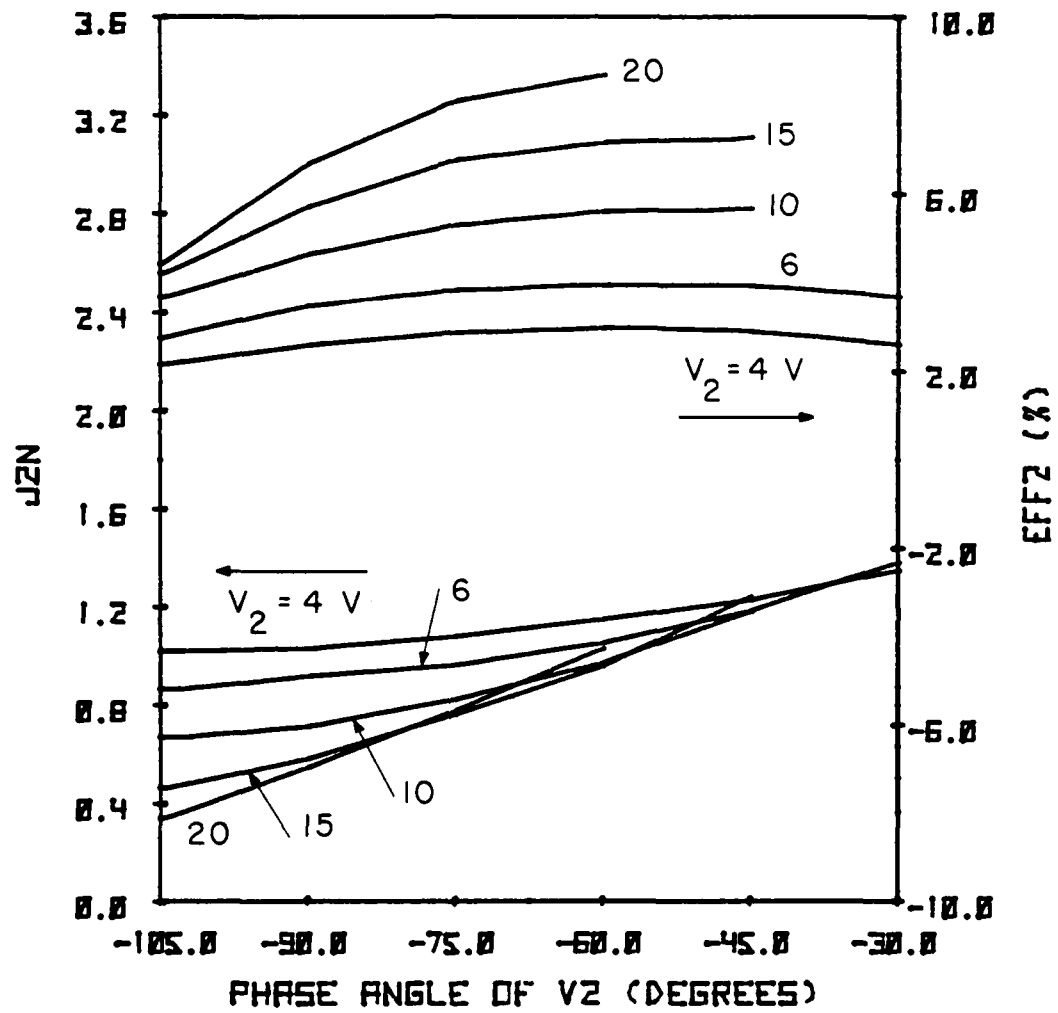
FIG. 2.44 J_{2N} AND Eff_2 VS. θ_{2V} FOR A Si UNIFORM DIODE AT $V_1 = 64$ V.

with the value of 2.49 percent for Eff_3. The maximum second-harmonic efficiency achieved at various V_1 and V_2, denoted as Eff_{2max}, is plotted in Fig. 2.45. From the figure, Eff_{2max} monotonically increases with V_2 and V_3 and never shows saturation in the voltage range indicated in this figure. The optimum second-harmonic efficiency is 10.96 percent at $V_1 = 65.8$ V, $V_2 = 20$ V, and $\theta_{2V} = -60$ degrees.

   2.3.4c Calculation of Harmonic Power Output. In order to calculate harmonic power output for the diodes investigated, the diode area must be determined by taking into account circuit matching and thermal effects. At first, third-harmonic power is calculated neglecting thermal effects. The diode area is chosen such that diodes can match 1 Ω of circuit resistance at the third harmonic. Thus the diode area is given by

$$A = - \frac{G_{d3}}{G_{d3}^2 + B_{d3}^2} = - R_{d3} \ , \qquad (2.50)$$

where G_{d3}, B_{d3} and R_{d3} are device conductance, susceptance, and resistance at the third-harmonic, respectively. Based on the results shown in Figs. 2.29, 2.33, 2.37, and 2.41, Tables 2.5 and 2.6 present the calculated third-harmonic power output together with some large-signal results. In the tables against each fundamental voltage, the first row lists calculated results for the maximum third-harmonic power point and the second row lists the calculated results for the maximum harmonic efficiency point. One interesting aspect that can be seen from the tables is that the diodes cannot deliver as much third-harmonic power at the maximum third-efficiency point as at the maximum third-harmonic power point. This means that, in terms of
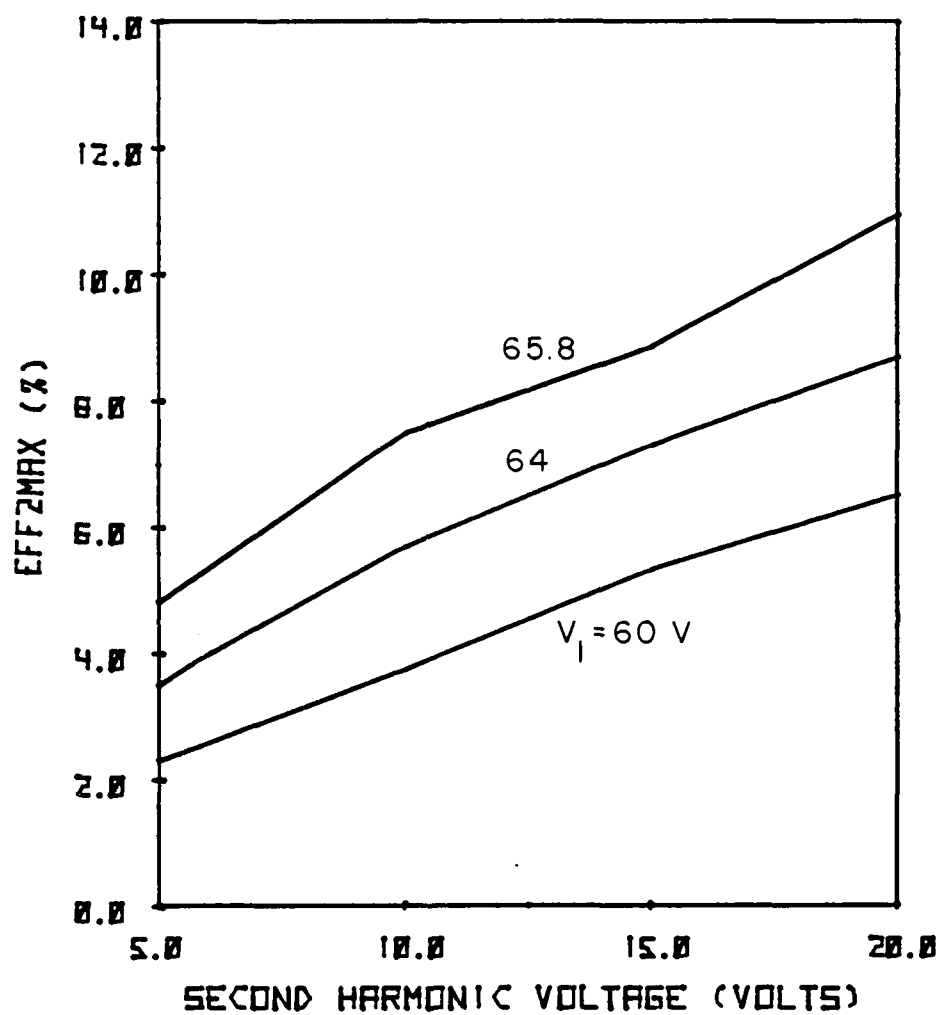
FIG. 2.45   MAXIMUM Eff$_2$ VS. SECOND-HARMONIC VOLTAGE AT
DIFFERENT FUNDAMENTAL VOLTAGES FOR A Si UNIFORM
DIODE.

Table 2.5

Third-Harmonic Power Generation of GaAs Diodes Obtained by Matching to 1-Ω Resistance (f_1 = 23 GHz)

(a) GaAs Read Diode

V_1 (V)	V_3 (V)	V_{dc} (V)	R_{d1} (Ω)	R_{d3} (Ω)	A (10^{-4} cm²)	Eff_1 (%)	Eff_3 (%)	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
33.0	2.0	41.7	-0.6	-1.0	0.53	24.03	1.17	2.8	0.032	3.2	97.6
33.0	4.0	41.9	-2.0	-1.0	0.16	22.53	1.67	0.8	0.014	1.8	323.9
32.6	1.0	39.3	-0.0	-1.0	1.77	0.10	1.33	8.6	0.115	5.9	23.7
32.6	1.0	39.3	-0.0	-1.0	1.77	0.10	1.33	8.6	0.115	5.9	23.7
32.4	1.0	40.5	-0.1	-1.0	1.10	9.99	1.10	5.4	0.060	4.7	41.7
32.4	1.0	40.5	-0.1	-1.0	1.10	9.99	1.10	5.4	0.060	4.7	41.7
32.2	1.0	42.5	-0.5	-1.0	0.70	25.67	0.49	3.7	0.018	3.7	74.5
32.2	3.0	42.3	-2.2	-1.0	0.15	21.47	0.93	0.8	0.007	1.7	335.6
32.0	1.0	42.8	-0.8	-1.0	0.51	26.46	0.38	2.7	0.010	3.2	101.6
32.0	6.0	43.1	-13.2	-1.0	0.03	28.96	0.73	0.2	0.001	0.8	1667.0

(b) GaAs Uniform Diode

V_1 (V)	V_3 (V)	V_{dc} (V)	R_{d1} (Ω)	R_{d3} (Ω)	A (10^{-4} cm²)	Eff_1 (%)	Eff_3 (%)	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
38.0	2.0	39.9	-0.0	-1.0	2.28	0.50	2.59	27.3	0.708	6.7	7.6
38.0	4.0	39.5	-0.0	-1.0	0.78	1.27	3.74	9.3	0.349	3.9	22.8
37.4	2.5	40.9	-0.1	-1.0	1.04	3.57	2.95	13.5	0.398	4.5	16.0
37.4	4.5	40.3	-0.1	-1.0	0.57	2.94	4.16	7.2	0.298	3.4	30.3
37.0	2.0	41.7	-0.2	-1.0	1.21	9.25	2.22	15.7	0.350	4.9	14.5
37.0	5.0	40.5	-0.2	-1.0	0.44	4.92	4.02	5.5	0.223	3.0	40.0
36.0	1.5	42.7	-0.3	-1.0	1.38	14.78	1.46	17.7	0.259	5.2	13.6
36.0	6.0	40.8	-0.3	-1.0	0.26	3.27	3.74	3.3	0.122	2.3	56.4
34.0	2.0	43.3	0.6	-1.0	0.87	18.62	1.27	11.3	0.150	4.2	21.3
34.0	5.0	42.7	-1.9	-1.0	0.21	13.85	2.66	2.7	0.072	2.0	89.3

Table 2.6

Third-Harmonic Power Generation of Si Diodes Obtained by Matching to 1-Ω Resistance (f_1 = 23 GHz)

(a) Si Hybrid Diode

V_1 (V)	V_3 (V)	V_{dc} (V)	R_{d1} (Ω)	R_{d3} (Ω)	A (10^{-4} cm^2)	Eff_1 (%)	Eff_3 (%)	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
51.0	2.0	64.4	-0.0	-1.0	2.86	1.60	1.13	29.9	0.338	7.5	6.9
51.0	2.0	64.4	-0.0	-1.0	2.86	1.60	1.13	29.9	0.338	7.5	6.9
50.0	2.0	68.4	-0.3	-1.0	2.58	16.31	0.91	27.4	0.250	7.1	8.9
50.0	6.0	64.2	-0.2	-1.0	0.59	3.48	2.12	6.1	0.129	3.4	35.2
48.0	2.0	72.2	-0.8	-1.0	1.56	25.54	0.59	17.3	0.105	5.6	15.4
48.0	7.0	72.3	-5.1	-1.0	0.28	27.42	1.15	3.2	0.037	2.4	88.1
44.0	1.0	73.6	-0.9	-1.0	1.95	26.64	0.19	23.3	0.043	6.2	11.8
44.0	7.0	73.7	-9.2	-1.0	0.19	27.54	0.77	2.2	0.017	1.9	127.1

(b) Si Uniform Diode

V_1 (V)	V_3 (V)	V_{dc} (V)	R_{d1} (Ω)	R_{d3} (Ω)	A (10^{-4} cm^2)	Eff_1 (%)	Eff_3 (%)	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
65.4	3.0	69.3	-0.0	-1.0	3.56	0.26	1.89	59.0	1.116	8.4	3.5
65.4	7.0	68.8	-0.0	-1.0	1.07	0.14	3.10	17.6	0.545	4.6	11.9
65.0	2.0	70.8	-0.1	-1.0	3.70	5.58	1.29	62.5	0.805	8.5	3.5
65.0	7.0	70.1	-0.2	-1.0	0.98	5.36	2.85	16.5	0.471	4.4	13.3
64.0	3.0	73.2	-0.2	-1.0	2.77	15.90	1.53	48.5	0.742	7.4	5.0
64.0	8.0	71.3	-0.6	-1.0	0.61	8.29	2.50	10.3	0.258	3.5	21.9
62.0	3.0	75.2	-0.5	-1.0	2.15	21.06	1.28	37.5	0.431	6.5	6.9
62.0	7.0	75.2	-1.5	-1.0	0.72	22.41	1.98	12.6	0.249	3.3	21.2
54.0	1.0	78.6	-0.5	-1.0	3.66	27.07	0.25	66.8	0.165	8.5	4.2
54.0	7.0	79.0	-4.8	-1.0	0.41	27.50	1.03	7.4	0.076	2.3	38.1
51.0	2.0	79.8	-1.5	-1.0	1.61	26.87	0.32	31.5	0.102	5.6	8.8
51.0	9.0	79.7	-10.9	-1.0	0.21	27.22	0.84	4.0	0.034	2.0	70.0

third-harmonic power, it is better to operate the diodes at low third-harmonic voltages. It was known from the previous discussions that, for a fixed V_1, third-harmonic current always decreases with increasing third-harmonic voltage. Consequently, the negative device third-harmonic resistance is a decreasing function of third-harmonic voltage. This leads to the decrease of third-harmonic power with increasing third-harmonic voltage. However, third-harmonic efficiency is independent of device area $(- R_{d3})$ so it can increase until saturation occurs.

Another interesting point is that the expected third-harmonic power, except that of the GaAs Read diode, becomes higher at higher V_1. Hence it is preferable to take advantage of depletion-layer modulation to enhance the third-harmonic power output. R_{th} listed in the tables is the thermal resistance required to keep the diode temperature below 500°K.

The tables indicate that the Si uniform diode can deliver a maximum third-harmonic power of 1.116 W, but at the optimum third-harmonic efficiency condition, it can only deliver 0.545 W. The Si hybrid diode can produce a maximum third-harmonic power of 0.338 W compared with the value of 0.125 W at the optimum third-harmonic efficiency condition. The GaAs Read diode can achieve a maximum third-harmonic power of 0.115 W compared with 0.014 W at the optimum third-harmonic efficiency condition. The GaAs uniform diode can generate a maximum third-harmonic power of 0.708 W compared with the value of 0.298 W at the optimum third-harmonic efficiency condition. It is concluded that, without considering thermal effects, the Si uniform diode outperforms the other diodes in terms of third-harmonic

power generation. This is partly due to the fact that the Si uniform diode has a higher impedance level, which is associated with its long device length and high third-harmonic current generation.

Although Tables 2.5 and 2.6 are estimates of the maximum third-harmonic power generating capabilities of diodes at different V_1, not all the values can be achieved in practice under CW conditions if thermal effects are taken into consideration. For thermal considerations, the maximum diode safe operating temperature of 500°K is assumed. This condition may not be met with an arbitrary diode area. Hence, the following analysis demonstrates the restrictions imposed on diode area and maximum achievable third-harmonic power for the diodes under CW conditions.

A simplified diode and heat sink structure[81] used for thermal considerations is given in Fig. 2.46. It is assumed that thermal contacts between metallic layers are ideal and all the heat flows through the bottom contact to the infinite half-space heat sink. The thermal resistance for a circular diode with a diameter D is given by

$$R_{th} = \frac{2}{\pi k_{hs} D} + \frac{4}{\pi D^2} \left(\frac{t_t}{k_t} + \frac{t_g}{k_g} + \frac{t_p}{k_p} \right) + \frac{4 t_1}{\pi D^2 k_1} + \frac{1.6 t_2}{\pi D^2 k_2} \quad , \quad (2.51)$$

where k_{hs} is the thermal conductivity of the heat sink and the other symbols are defined in Fig. 2.46. The first term in the preceding equation gives the thermal spreading resistance for the infinite half-space heat sink. This term, adopted from the report by Mains and Haddad,[73] is the result obtained by Kennedy[82] for the case of a uniform current heat flux incident on a large cylindrical heat sink. Diamond and copper heat sinks are used. The thermal conductivities
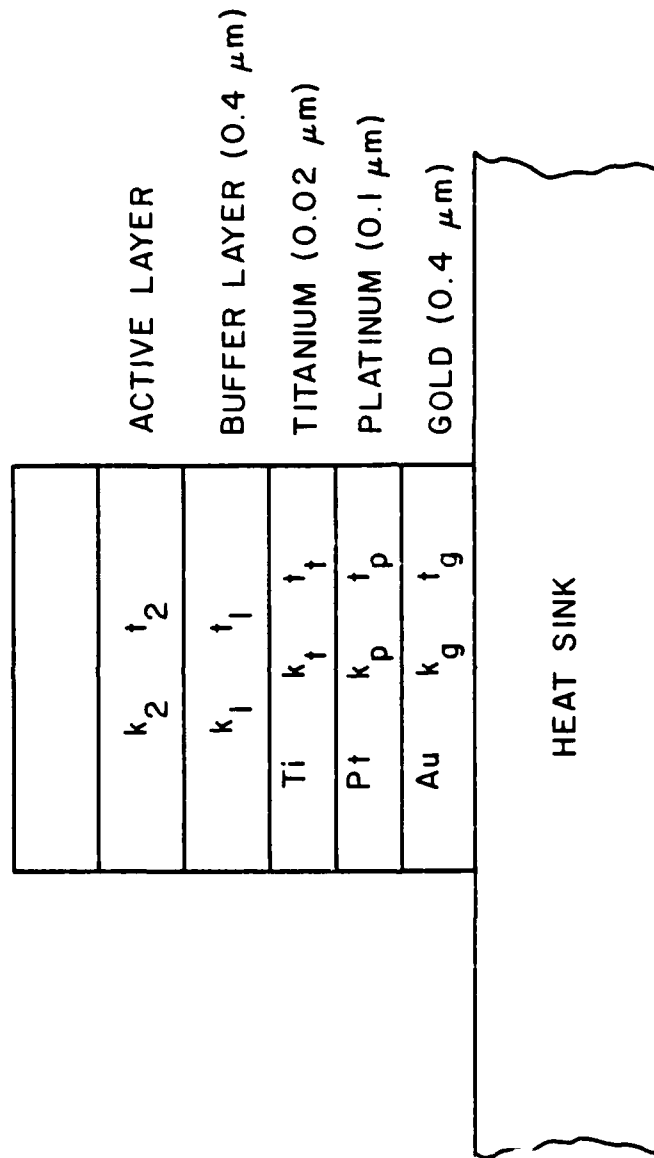
FIG. 2.46 A SIMPLIFIED DIODE AND HEAT SINK STRUCTURE.

of diamond and copper are 11.7 and 3.9 W/cm-°C, respectively. A ring geometry is used to reduce the value of the first term. As explained in Reference 73, improvement by a factor of 0.55 is used for this term.

The terms in parentheses of Eq. 2.51 are contributed from the metallization layers for ohmic contact purposes. The layer thickness and thermal conductivities of the layers are indicated in Fig. 2.46. The third term in the equation is the thermal resistance of the buffer layer with a thickness of 0.4 µm. In this term k_1 is the thermal conductivity of either Si or GaAs. The thermal conductivity for GaAs is expressed as

$$k_{GaAs} = 120/T \ \ W/cm\text{-}°C \ ,$$ (2.52)

where T is the average temperature of the buffer layer. As is explained in Reference 73, Eq. 2.52 agrees with the expression given by Olson[83] and also with the experimental conductivity data of Maycock.[84] Also pointed out in the same reference, the thermal conductivity of Si in the interesting temperature range is approximately three times that of GaAs. Therefore, the thermal conductivity of Si is

$$k_{Si} = 360/T \ ,$$ (2.53)

where T, the average buffer layer temperature, is assumed to be 450°K throughout the calculation.

The last term in Eq. 2.51 is the thermal resistance of the active layer, which has the same form as the previous term but is reduced by a factor of 0.4 for taking into account the nonuniform heat

generation in the diode. t_2 is taken to be equal to the p-layer thickness. Restriction in diode diameter for the temperature not to exceed 500°K can be found by the following inequality:

$$R_{th}(1 - Eff_1 - Eff_3)V_{dc}J_{dc} \frac{D^2}{4} \leqq 202 \ . \qquad (2.54)$$

The diode diameter is also restrained by

$$\frac{\pi D^2}{4} \leqq - R_{d3} \ . \qquad (2.55)$$

By taking the equal sign for these two equations to calculate D and choosing the minimum one from the calculated diameter, the maximum achievable third-harmonic power can be estimated.

Based on the data shown in Figs. 2.29, 2.33, 2.37, and 2.41, the overall maximum third-harmonic power for the diodes with different heat sinks is listed in Table 2.7. For a single mesa on a copper heat sink, except that of the GaAs Read diode, third-harmonic power is thermally limited. The GaAs uniform diode can achieve the highest third-harmonic power of 0.403 W, and the corresponding efficiency is also the highest. For a single mesa on a diamond heat sink, the third-harmonic power for each diode is electronically limited. The Si uniform diode outperforms other diodes in terms of power. It can achieve the highest third-harmonic power of 1.16 W but the GaAs uniform diode still has the highest efficiency. For a ring geometry on a copper heat sink, only the Si uniform diode is thermally limited in power but it can deliver the highest third-harmonic power of 0.819 W. The GaAs uniform diode can achieve a third-harmonic power of 0.708 W with an efficiency a little higher than that of the Si uniform diode. For a ring geometry on a diamond heat sink,

Table 2.7

CW Results for Third-Harmonic Performance of Si and GaAs Diodes Taking

into Account the Thermal Effect (f_1 = 23 GHz)

(CM = a single mesa on a copper heat sink, DM = a single mesa on a diamond heat sink, CR = a ring

geometry on a copper heat sink, DR = a ring geometry on a diamond heat sink, GR = GaAs Read diode,

GU = GaAs uniform diode, SH = Si hybrid diode, SU = Si uniform diode)

Diode – Heat Sink	V_1 (V)	V_3 (V)	θ_{3V} (V)	I_{dc} (A)	P_{dc} (W)	Eff_1 (%)	Eff_3 (%)	R_{d1} (Ω)	R_{d3} (Ω)	P_3 (W)	D (mils)	R_{th} (°C/W)
CM – GR	32.6	1.0	20.0	0.22	8.65	0.10	1.33	-0.00	-1.00	0.115	5.9	12.8
CM – GU	38.0	3.5	20.0	0.28	10.91	0.50	3.69	-0.01	-1.16	0.403	4.1	19.3
CM – SH	50.0	2.0	10.0	0.32	22.23	16.31	0.91	-0.33	-1.23	0.203	6.4	11.0
CM – SU	64.0	7.0	20.0	0.18	12.91	15.68	2.42	-0.90	-1.16	0.313	3.8	19.1
DM – GR	32.6	1.0	20.0	0.22	8.65	0.10	1.33	-0.00	-1.00	0.115	5.9	5.6
DM – GU	38.0	2.0	20.0	0.69	27.35	0.50	2.59	-0.00	-1.00	0.708	6.7	4.7
DM – SH	51.0	2.0	10.0	0.46	29.88	1.60	1.13	-0.02	-1.00	0.338	7.5	3.6
DM – SU	65.4	3.0	10.0	0.85	58.97	0.26	1.89	-0.00	-1.00	1.116	8.4	3.0
CR – GR	32.6	1.0	20.0	0.22	8.65	0.10	1.33	-0.00	-1.00	0.115	5.9	8.0
CR – GU	38.0	2.0	20.0	0.69	27.35	0.50	2.59	-0.00	-1.00	0.708	6.7	6.7
CR – SH	51.0	2.0	10.0	0.46	29.83	1.60	1.13	-0.02	-1.00	0.338	7.5	5.4
CR – SU	65.4	5.0	10.0	0.46	32.43	5.23	2.53	-0.11	-1.00	0.819	6.1	6.7
DR – GR	32.6	1.0	20.0	0.22	8.65	0.10	1.33	-0.00	-1.00	0.115	5.9	4.0
DR – GU	38.0	2.0	20.0	0.69	27.35	0.50	2.59	-0.00	-1.00	0.708	6.7	3.2
DR – SH	51.0	2.0	10.0	0.46	29.88	1.60	1.13	-0.02	-1.00	0.338	7.5	2.3
DR – SU	65.4	3.0	10.0	0.85	58.97	0.26	1.89	-0.00	-1.00	1.116	8.4	1.9

all the diodes have the same performance as the case of a single

mesa on a diamond heat sink.

Overall, the Si uniform diode shows higher third-harmonic

power than the other diodes, except for the case of a single mesa

on a copper heat sink, but the GaAs uniform diode achieves higher

third-harmonic efficiency.

When the same procedure for calculation of the third-harmonic

power is used, the second-harmonic power for the Si uniform diode can

be estimated. Table 2.8 presents the results for the maximum second-

harmonic power and the power at the maximum second-harmonic efficiency

point for each V_1. It is seen in the table that the maximum second-

harmonic power still occurs at low second-harmonic voltages. The

maximum second-harmonic power is 2.591 W at V_1 = 65.8 V and V_2 = 5 V.

Table 2.9 indicates the maximum second-harmonic power for

different heat sink structures. The diode can achieve higher second-

harmonic power in a diamond heat sink.

2.3.5 Summary and Conclusions. The harmonic power generation

properties of several IMPATT diodes were studied. These properties

are affected by avalanche multiplication, the drift process, and

depletion-layer modulation. From single-frequency operation, avalanche

multiplication was found to be important for the formation of the

injected current. However, for all the diodes investigated, the

harmonic current before depletion-layer modulation occurs is much

smaller than the fundamental current, even though the injected current

waveform becomes sharper at higher terminal RF voltages. This

suggests that the drift process, required to delay the injected

particles for collection, degrades harmonic current generation at

Table 2.8

CW Results for Second-Harmonic Performance of the Si Uniform Diode

Obtained by Matching 1-Ω Resistance (f_1 = 23 GHz)

V_1 (V)	V_2 (V)	V_{dc} (V)	R_{d1} (Ω)	R_{d2} (Ω)	A (10^{-4} cm^2)	Eff_1 (%)	Eff_2 (%)	P_{dc} (W)	P_2 (v)	D (mils)	R_{th} (°C/W)
60.0	5.0	77.1	-0.4	-1.0	3.49	24.96	2.31	62.7	1.446	8.3	4.4
60.0	20.0	78.3	-1.4	-1.0	0.64	15.27	6.53	12.0	0.782	3.6	21.6
64.0	6.0	75.3	-0.3	-1.0	3.34	18.29	4.00	61.1	2.444	8.1	4.3
64.0	20.0	76.6	-0.7	-1.0	0.84	10.85	8.71	15.3	1.377	4.1	15.9
65.8	5.0	71.9	-0.0	-1.0	3.20	3.30	4.81	53.9	2.591	7.9	4.1
65.8	20.0	74.8	-0.2	-1.0	0.98	4.25	10.95	17.6	1.923	4.4	13.5

Table 2.9

CW Results for Second-Harmonic Performance of the Si Uniform Diode

Taking into Account the Thermal Effects (f_1 = 23 GHz)

Diode Heat Sink	V_1 (V)	V_2 (V)	θ_{2V} (Deg.)	I_{dc} (A)	P_{dc} (W)	Eff_1 (%)	Eff_2 (%)	R_{d1} (Ω)	R_{d2} (Ω)	P_2 (W)	D (mils)	R_{th} (°C/W)
CM - SU	65.3	20.0	-60.0	0.15	11.39	4.25	10.96	-0.31	-1.55	1.248	3.5	20.9
DM - SU	65.3	5.0	-60.0	0.75	53.90	3.30	4.81	-0.04	-1.00	2.591	7.9	3.2
CR - SU	65.8	10.0	-45.0	0.46	33.95	3.44	7.50	-0.07	-1.00	2.548	6.2	6.5
DR - SU	65.8	5.0	-60.0	0.75	53.90	3.30	4.81	-0.04	-1.00	2.591	7.9	2.0

low voltages. In other words, without depletion-layer modulation,

diodes may not be good for harmonic power generation.

At high RF voltages, depletion-layer modulation causes a

change in diode performance. The effects of depletion-layer modula-

tion depend on the doping profile and v-E characteristics of carriers.

Low doping concentration, as in the GaAs Read diode, results in a

rapid increase of harmonic current with voltage level. It was found

that both Si and GaAs uniform diodes in single-frequency operation can

produce higher harmonic current than the other diodes. However, the

phase angle of harmonic current in both diodes is different because

of the different v-E characteristics of carriers in Si and GaAs.

Operating diodes at a high fundamental voltage is necessary for

high harmonic power generation. An appropriate harmonic voltage can

delay the onset of depletion-layer modulation and keep the diode in

active mode operation. It is found for third-harmonic performance

that the third-harmonic voltage will cause a decrease in third-

harmonic current and an increase in phase delay of the third-harmonic

current. This makes the third-harmonic efficiency saturate at high

third-harmonic voltages and restrains third-harmonic power generation

of diodes. The GaAs uniform diode can achieve the highest third-harmonic

efficiency of 4.1 percent because this diode has a high third-harmonic

current generation and small phase delay in the third-harmonic

current. With considerations of circuit match and thermal effects,

the Si uniform diode can achieve more third-harmonic power than the

other diodes, since this Si diode has a longer device length.

For second-harmonic performance, the Si uniform diode can

achieve a second-harmonic efficiency of 10.96 percent. This is

because a high second-harmonic voltage can be applied to the
terminal without causing the terminal voltage to vary too fast.
For thermal and circuit-matching considerations the diode can
achieve a second-harmonic power of 2.591 W.

In conclusion, better harmonic performance can be   achieved
in a highly doped IMPATT diode because of moderate depletion-layer
modulation. The uniform structure becomes the best structure for
harmonic power generation because high doping concentration is easily
achieved. It is expected for a uniform double-drift IMPATT diode that
harmonic performance can be improved if the punch-through factor in
the n-side is appropriate. It is unlikely that the punch-through
factor in the p-side will be kept close to one because the mobility
of holes is low, compared with those of electrons. Too high a doping
on the n-side is also prohibitive since depletion-layer modulation
will not be significant enough to cause the induced current dip. It
is better to keep the doping concentrations on the n- and p-sides as
close as possible such that depletion-layer modulation can occur on
both sides at nearly the same time.

As far as depletion-layer modulation is concerned, space-
charge effects may not degrade harmonic performance as much as
fundamental performance. It is expected that pulsed mode $\smile_{\varepsilon}$ .ation
can yield more harmonic power with reasonable harmonic effic .ncy.

2.4 pin Diodes as Frequency Multipliers

2.4.1 Introduction. Pin diodes operating in avalanche break-
down are studied for their capabilities in frequency-multiplication
applications. In this study, the diodes are considered in the passive

mode of operation, which means that the diode is driven by an external fundamental source and the harmonic power is extracted from it. This type of operation for the pin diode was discussed by Ntake and Conn.[85] Their theoretical analysis only applied the method given by Burckhart[86] and Scanlan[87] to the case of a diode overdriven in the reverse-avalanche region by taking into account an avalanche inductance. Their theory leads to inaccurate prediction of the performance under a large reverse-overdriven condition because of the neglect of space-charge and transit-time effects. However, their experimental results for a 2- to 6-GHz frequency multiplier were encouraging and a measured conversion efficiency of 73 percent was achieved.

Under avalanche breakdown, a pin diode has no avalanche-free drift region and avalanche multiplication occurs throughout the entire space-charge layer. According to a small-signal analysis in single-frequency operation, Misawa[88] pointed out that the cutoff frequency of the diode goes to dc due to the intrinsic instability of the electron-hole plasma over the entire space-charge region. Hence, the negative resistance of the diode is extremely broadband and peaks in the vicinity of the avalanche resonance frequency. Compared at the same operating conditions, the magnitude of negative resistance of the diode is lower than that of a Read structure.

It is the purpose of this section to investigate the large-signal behavior of pin diodes in single- and multifrequency operation utilizing a full-scale simulation. For simplicity, only the fundamental and third-harmonic signals are considered. Simulation results for the diodes at different dc current densities are compared in

terms of their fundamental and third-harmonic current generation

capabilities. Moreover, the effects of the terminal voltage on

the injected and induced currents are discussed to determine the

optimum conditions for achieving high third-harmonic current.

Practical considerations, such as circuit matching and thermal

effects, are included to evaluate the third-harmonic power output

and the conversion efficiency. Throughout this investigation, no

specific attention is paid to depletion-layer modulation since this

modulation no longer occurs in most situations.

2.4.2 Comparison of a pin Diode with a Varactor Diode in
Frequency Multiplication. Harmonic power generation or frequency multi-
plication can be achieved by using any nonlinear device pumped with an

external fundamental source. The most often used device for this pur-

pose is a varactor diode that has a nonlinear capacitance. A pin

diode is considered to be an alternative candidate due to its non-

linear avalanche multiplication. Despite the different nonlinear mech-

ansims employed, both diodes are operated at different bias conditions.

The varactor diode is usually reverse biased with a dc voltage less

than the breakdown value, while the pin diode is biased at breakdown

with a dc current flowing through it.

According to Manley-Rowe relations, a lossless varactor diode

can achieve 100-percent conversion from the fundamental to a harmonic

frequency. However, with a series resistance which is inherent to a

varactor, the conversion efficiency may be much lower because of the

dissipation of useful power. On the other hand, in a practical

varactor diode, the conversion efficiency is strongly dependent on

the ratio of device reactance to device resistanc . When this ratio

is kept high, the conversion efficiency can be close to the ideal value, otherwise the efficiency is degraded. For example, in an abrupt-junction varactor diode, Penfield[89] indicated that a tripler employing this diode, with an input frequency around $0.04\,\omega_c$ where ω_c is the cutoff frequency, may achieve a conversion efficiency of approximately 30 percent. In addition, several factors, such as power dissipation, dc breakdown voltage and maximum capacitance swing, will limit the maximum harmonic power generation from the diode.

A pin diode may achieve a conversion efficiency higher than 100 percent because of the role of the dc power. It is known that the Manley-Rowe relations are only valid for a lossless nonlinear reactance element without dc power consumption. These relations do not apply to the pin diode, in which RF power can be self-generated with a supply of dc power. Under appropriate conditions, the dc power can aid the conversion from input power to output power. In comparison with a varactor diode, the pin diode has the following advantages:

1. There is no series resistance in the pin diode, except for the contact resistance, to degrade the conversion efficiency.

2. The maximum swing of the terminal voltage is approximately equal to the dc voltage, while in a varactor diode the maximum terminal voltage swing is less than half the dc breakdown voltage.

3. The harmonic power can be enhanced by increasing the dc power until thermal limitations set in.

4. Fabrication for the pin diode is much easier than for a varactor diode. However, the pin diode has an inherent dc instability

due to its negative resistance at low frequencies, and a complicated
bias circuit is needed to suppress this instability.

The harmonic power generation capability of the pin diode is
limited by several factors: (1) The harmonic current amplitude is
always less than twice the dc current since no depletion-layer modula-
tion can occur to make the induced current become negative. (2) The
dependence of avalanche build-up time and transit time on the device
length affects the formation of the injected and induced currents.
A short device length can reduce the build-up time to improve the
injected and induced current waveforms, but the device impedance level
is decreased. Hence, a trade off is necessary to determine the
optimum harmonic power output. In spite of these limitations, the pin
diode offers an alternative way to generate harmonic power.

2.4.3 Design Considerations for pin Diodes. Si is chosen as
the semiconductor material needed for the design of pin diodes. The
choice of Si rather than GaAs is based on its physical property. Si
has highly nonlinear ionization rates that show signs of saturation
at a field higher than 0.8 MV/cm and high carrier velocities at
$T = 500°K$ as compared to GaAs. Hence, the Si pin diode is expected
to have a higher third-harmonic current generation since it can have
a sharp induced current waveform. In addition, the thermal conduc-
tivity of Si is three times higher than GaAs, so the Si pin diode
can be biased with a high dc current density to enhance harmonic
power output.

The diode structure is shown in Fig. 2.47. The intrinsic
region width is 1.2 μm for pin diode 1, 0.6 μm for pin diode 2, and
1.8 μm for pin diode 3, respectively. The width of pin diode 3 is
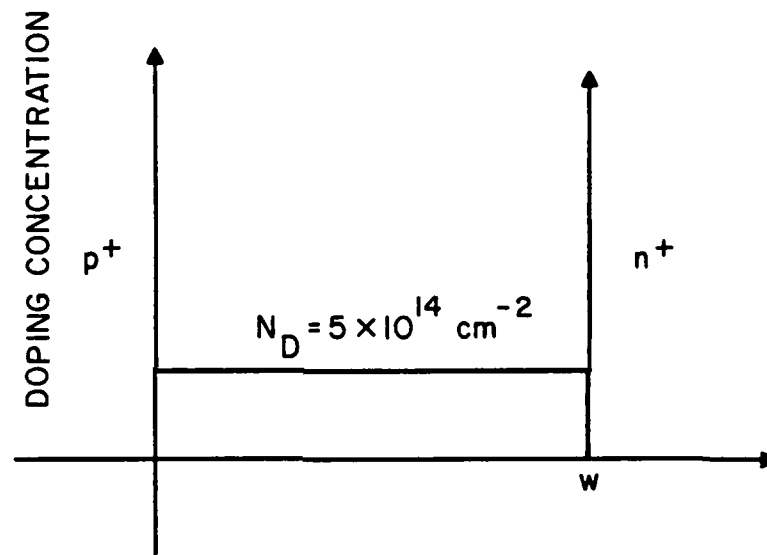
fig. 2.47 DOPING CONCENTRATION OF A pin DIODE.

approximately the same as that of a single-drift Read IMPATT diode operating optimally at 23 GHz with a transit angle of 0.74π and with an avalanche region width of 0.3 μm. The intrinsic region of each pin diode is lightly doped with $N_d = 5 \times 10^{14}$ cm³. Throughout the simulation the device temperature is 500°K and the material parameters are the same as those in Table 2.1

2.4.4 Brief Description of Small-Signal Analysis for pin Diodes.

A small-signal analysis is carried out in order to understand the properties of a pin diode under avalanche-breakdown conditions and, more specifically, the property of a pure avalanche region. The incremental negative resistance of a pin diode under small-signal conditions can be predicted only by Misawa's approach rather than by the standard Read-type approach. The major difference between these two approaches lies in the way of dealing with the conduction current in the avalanche region. The Read-type approach makes an assumption of constant conduction current, i.e., independent of position. Using this assumption and writing Maxwell's equation for the magnetic field as

$$\nabla \times H = J_c + \varepsilon \frac{\partial E}{\partial t} \qquad (2.56)$$

and applying the identity

$$\nabla \cdot \nabla \times H = 0 \qquad (2.57)$$

yields the following for the one-dimensional case:

$$\frac{\partial}{\partial x} \frac{\partial}{\partial t} (\varepsilon E) = 0 \; . \qquad (2.58)$$

Interchanging the order of differentiation in the preceding equation gives

$$\frac{\partial}{\partial t} \frac{\partial}{\partial x} (\epsilon E) = \frac{\partial}{\partial t} q[N_B(x) + p(x,t) - n(x,t)] \quad . \qquad (2.59)$$

Equation 2.59 indicates that the assumption of constant conduction current in the avalanche region implies that the shape of the electric field in the avalanche region is independent of time. Thus, a physical interpretation of this is that the time dependence field produced by space charge within the avalanche region is neglected. Strictly speaking, this assumption is not quite right, and will lead to an error of 20 percent in the avalanche resonance frequency.[90] Furthermore, the avalanche region can be modeled only by a capacitance in parallel with an inductance from the Read approach. When the space-charge effect is taken into account, Misawa's approach leads to a negative resistance in the avalanche region. While equal ionization rates and drift velocities are assumed for electrons and holes, Poisson's equation and the continuity equation for the small ac parts can be expressed as follows:

$$\frac{d\tilde{E}}{dx} = \frac{1}{\epsilon v_s} (\tilde{J}_n - \tilde{J}_p) \quad , \qquad (2.60)$$

$$\frac{d\tilde{J}_n}{dx} = \alpha_o (\tilde{J}_n + \tilde{J}_p) + \alpha'\tilde{E}J_{dc} - \frac{j\omega}{v_s} \tilde{J}_n \qquad (2.61)$$

and

$$\frac{d\tilde{J}_n}{dx} = - \alpha_o (\tilde{J}_n + \tilde{J}_p) - \alpha'\tilde{E}J_{dc} + \frac{j\omega}{v_s} \tilde{J}_p \quad , \qquad (2.62)$$

where α_o is the ionization rate at the dc field and the tilda indicates the small ac signal. The requirement that the total ac current be independent of position leads to

$$\tilde{J}_t = \tilde{J}_n + \tilde{J}_p + j\omega\varepsilon\tilde{E} = \text{const} . \tag{2.63}$$

With this requirement, the impedance of a pin diode can be derived. No matter what the diode dimension is, the diode exhibits a negative-resistance property for all the frequencies.

2.4.5 Performance of pin Diodes in Single-Frequency Operation.

This section focuses on the large-signal performance of pin diodes in single-frequency operation. To achieve this, computer simulations were carried out for the diodes with three different dc current densities, namely, 3.6 kA/cm^2, 7.5 kA/cm^2 and 15 kA/cm^2. Device performance is compared in terms of space-charge and transit-time effects.

In conventional IMPATT diodes, space-charge effects can turn off avalanche multiplication prematurely and reduce the 90-degree phase delay provided by avalanche multiplication. As a result, the power generated at the optimum transit-time frequency is degraded. For most analytical methods that have been employed to study conventional IMPATT diodes, the effects of space charge in the drift region have been taken into account, but space-charge effects in the avalanche region have been neglected because of the assumption of a short avalanche region length. However, in pin diodes, the device length is long enough such that space-charge effects are not negligible. As discussed previously in the small-signal analysis, space-charge effects are responsible for negative resistance in pin diodes. For large-signal operation, space-charge and transit-time effects combine to change the electric field distribution; this will cause modulation of drift velocities of charge carriers, affect avalanche

multiplication, and give rise to a difference in performance under various conditions.

In the following discussions the injected and induced currents are treated separately because they are not simply related to one another. Strictly speaking, the injected current, according to Eq. 2.28 is a measure of instantaneous charge generated in the avalanche region. The generated charge is not immediately collected at the contacts of the pin diode due to finite transit time. The injected current can be considered to be the same as the induced current provided that the transit time is very small and the constant conduction current can be maintained. However, as pointed out in the small-signal analysis, the assumption of constant induction current is no longer valid in pin diodes and the injected and induced currents are not linearly related.

2.4.5a Performance of pin Diode 1. To investigate the effects of space charge on the performance of pin diode 1, large-signal solutions at V_1 = 32 V for three different dc current densities are shown in Fig. 2.48. A brief summary of certain characteristics of the injected current is presented in Table 2.10 where θ_p is the position of the injected current peak and θ_ω is the half width of the current. It can be seen from the table that increasing dc current causes the injected current shift to the left and makes the current widen slightly. As a result, the peak value of the current is not linearly proportional to the dc current density. When the dc current density increases, more charge is generated in the depletion region. The space-charge effect is enhanced in such a manner as to turn off avalanche multiplication earlier and
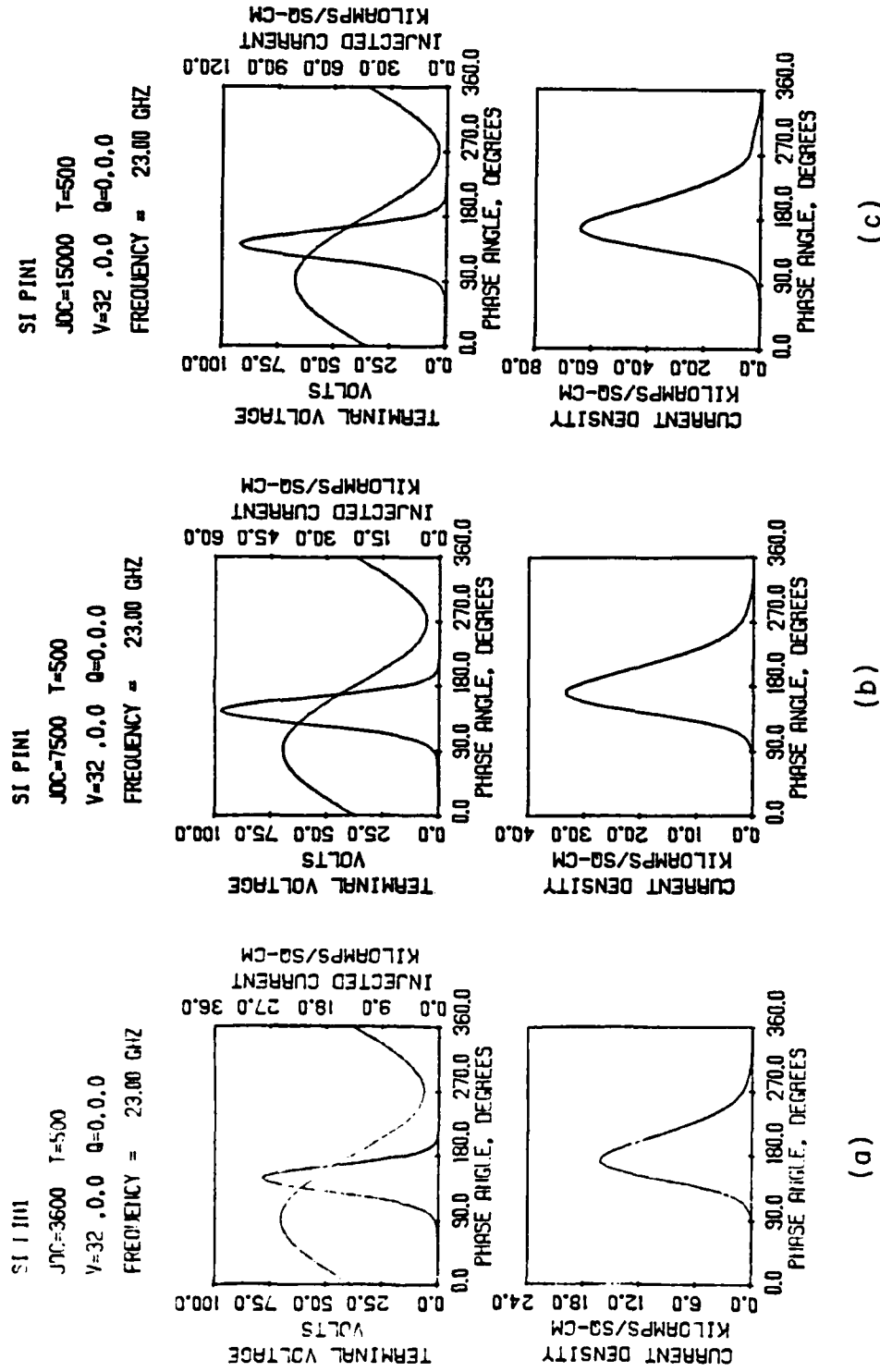
FIG. 2.48   LARGE-SIGNAL SOLUTIONS OF pin DIODE 1 AT V_1 = 32 V FOR THREE DIFFERENT dc CURRENT DENSITIES.

this results in the change in the injected current. Details on the space-charge effect on avalanche multiplication is discussed later.

Table 2.10

Summary of Characteristics of the Injected Current

of pin Diode 1 at $V_1 = 32$ V

J_{dc} (kA/cm^2)	J_{injm} (kA/cm^2)	θ_p (Degrees)	θ_ω (Degrees)
3.6	28.4	147.6	43.2
7.5	58.3	144	45
15	110	140.4	46.8

The induced current is also subject to some changes due to the increase of dc current density. As seen from Fig. 2.48, the induced current is not symmetric about its peak position. The current rises rapidly, but after reaching its peak, it does not drop off as fast. A brief summary about the induced current waveform shown in Fig. 2.48 is given in Table 2.11 where θ_L is distance between the peak position and the half-amplitude point in the rising edge of the induced current and $\theta_R = \theta_\omega - \theta_L$.

The induced current peak apparently shifts to the left with increasing dc current density as a consequence of the shift of the injected current. More precisely, the space-charge effect is responsible for the shift in the induced current. The slow fall off in the induced current implies that the transit-time effect also plays a dominant role in the induced current waveform. Although most charge carriers generated can be extracted within a typical transit time

Table 2.11

Summary of Characteristics of the Induced Current

of pin Diode 1 at V_1 = 32 V

J_{dc} (kA/cm^2)	J_{indm} (kA/cm^2)	θ_p (Degrees)	θ_L (Degrees)	θ_R (Degrees)	θ_ω (Degrees)
3.6	16.2	172.8	30.6	43.2	73.8
7.5	33.2	169.2	30.6	45	75.6
15	64.4	165.6	30.6	46.8	77.4

(i.e., device length/saturated velocity), some of the carriers remain

in the depletion region when the terminal RF voltage reaches its

minimum (ωt = 270 degrees). At this moment, the electric field is so

low that the carriers drift at very low velocities, since the drift

velocities of electrons and holes are monotonically increasing functions

of electric field. The induced current at this moment is relatively

higher for higher dc current densities. For instance, the induced

current is 4.52 kA/cm^2 for J_{dc} = 15 kA/cm^2, 2.2 kA/cm^2 for J_{dc} =

7.5 kA/cm^2, and 1.01 kA/cm^2 for J_{dc} = 3.6 kA/cm^2, respectively. This

means that there are relatively more carriers that remain in the

depletion region at ωt = 270 degrees. In other words, the velocity

modulation induced by the space-charge effect has an influence on

charge extraction.

The space-charge effect is investigated for the case of J_{dc} =

7.5 kA/cm^2 and V_1 = 32 V. Figure 2.49 displays the diode states at

three different instants in the RF cycle. At ωt = 144 degrees, the

terminal voltage is 18 V above the dc value. From Fig. 2.49, it is

seen that the generated charge carriers become significant and most

-154-
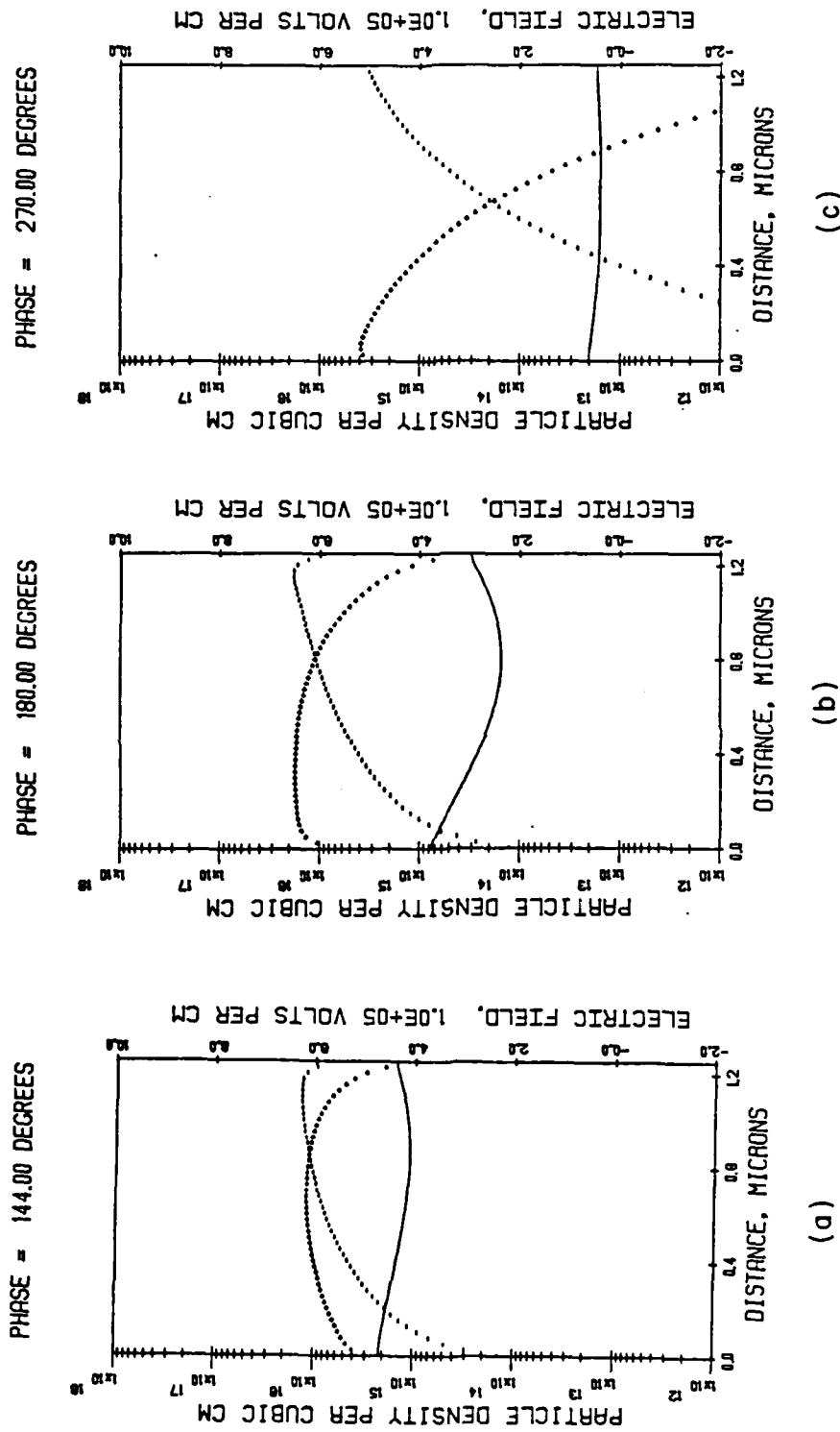
FIG. 2.49 STATE OF pin DIODE 1 AT THREE DIFFERENT INSTANTS FOR J_{dc} = 7.5 kA/cm^2 AND V_1 = 32 V.

of the charge carriers remain in the depletion region. Due to the
different characteristics of electrons and holes, the electron and
hole distributions are not similar throughout the entire depletion
region. The hole density rises quickly from the right edge of the
depletion region, but the electron density does not rise rapidly from
the left edge. There is a net excess of holes on the left side of
the region, and the positive charge in itself causes a decrease in the
electric field. Similarly, there is a net excess of electrons in the
right side of the region and this leads to an increase in the magnitude
of the electric field. As a consequence, the field is low in the
central portion of the region. Because of asymmetry between the
electron and hole distributions the electric field reaches its
minimum closer to the right edge and is higher at the left edge than
the right edge. The lowering of the field in the central portion, in
turn, reduces avalanche multiplication. However, the lowering at this
moment is not so significant as to eliminate avalanche multiplication.

At $\omega t = 180$ degrees, the electron and hole densities, shown in
Fig. 2.49b, increase little compared with those at $\omega t = 144$ degrees.
This indicates that avalanche multiplication is suppressed during the
interval between $\omega t = 144$ and 180 degrees. It can be seen that the
electron and hole carriers have moved to the right and left, respec-
tively. This movement enhances the net excess of holes in the left
side of the region and that of electrons in the right side of the
region. Therefore, the electric field is brought down further so
that the carriers in the central portion, particularly holes, move
more slowly than those near the edges. This delays the extraction
of the carriers in the central portion, and the lowering of the

electric field will reduce greatly the avalanche multiplication in this portion.

After $\omega t = 180$ degrees, carriers continue to move out of the depletion region for collection. The decrease in charge density due to collection tends to flatten the electric field distribution. However, the average electric field in the region is low due to the drop of the terminal voltage after that moment. At $\omega t = 270$ degrees, as shown in Fig. 2.49c, most carriers have been collected but some remain in the region. The number of carriers that remain depends on the velocity modulation that carriers in the central portion experience during the interval between $\omega t = 180$ and 270 degrees. It is obvious that for high J_{dc} the lowering of electric field in the central portion during this interval is significant and enhances velocity modulation. Consequently, more carriers will remain in the depletion region at $\omega t = 270$ degrees at higher dc current densities, and this results in a relatively higher induced current at this moment.

The space-charge effects are important for device performance. Table 2.12 presents the large-signal results for pin diode 1. The properties of the first three Fourier components of the induced current are illustrated in Fig. 2.50. From the figure, it is seen that as the normalized RF voltage increases from zero, the normalized fundamental current rises quickly due to the nonlinearity of ionization rates and tends to saturate at higher normalized RF voltages. This saturation phenomenon is partly related to the back-bias effect, which will prevent further increase in the maximum instantaneous electric field. The normalized fundamental current decreases slightly

Table 2.12

Large-Signal Results for pin Diode 1 in Single-Frequency Operation for Three Different dc Current Densities

V_1 (V)	V_{dc} (V)	J_{dc} (kA/cm²)	Eff (%)	P_1 (kW/cm²)	J_1 (A/cm²)	θ_{1I} (Deg.)	J_2 (A/cm²)	θ_{2I} (Deg.)	J_3 (A/cm²)	θ_{3I} (Deg.)
1.0	45.9	14953	0.04	0.3	2308	-103.2	72	92.7	9	179.3
5.0	45.8	15063	0.92	6.4	10826	-103.6	1622	82.3	153	-84.8
12.0	44.6	15015	3.08	20.7	19288	-100.3	6458	83.4	1618	-70.2
20.0	42.4	15374	4.58	29.3	23400	-97.3	11073	86.2	4173	-71.0
28.0	39.2	15067	4.38	25.8	24213	-94.4	13265	91.1	6069	-67.6
30.0	38.1	15297	3.82	22.3	24667	-93.5	13826	93.3	6579	-65.7
32.0	35.4	15285	-1.08	-5.8	24205	-89.1	14315	102.9	6917	-57.6
5.0	46.1	7541	0.83	2.9	5730	-101.4	1002	83.6	117	-77.8
12.0	45.0	7402	2.72	9.1	9976	-98.7	3760	83.3	1007	-77.5
20.0	43.0	7606	4.26	13.9	11938	-96.7	6152	84.4	2384	-79.1
28.0	40.0	7753	4.51	14.0	12797	-94.5	7413	88.2	3424	-75.4
30.0	39.0	7316	3.88	11.1	12141	-93.5	7193	90.2	3433	-73.3
32.0	37.6	7233	2.40	6.5	12019	-91.9	7265	93.7	3590	-69.7
33.0	35.9	7575	-0.80	-2.2	12499	-89.4	7689	99.6	3844	-63.9
1.0	46.4	3485	0.05	0.1	626	-103.8	26	106.5	7	173.5
5.0	46.2	3569	0.83	1.4	3879	-101.0	543	80.2	67	-84.7
12.0	45.3	3680	2.91	4.8	5101	-99.1	2015	80.1	548	-85.6
20.0	43.5	3556	5.07	7.8	5689	-97.9	3005	80.4	1168	-87.2
28.0	40.7	3638	5.91	8.7	6068	-95.9	3596	84.2	1659	-83.1
30.0	39.7	3691	5.53	8.1	6185	-95.0	3731	86.2	1779	-80.7
32.0	38.4	3540	4.38	6.0	5942	-93.6	3647	89.4	1801	-77.0
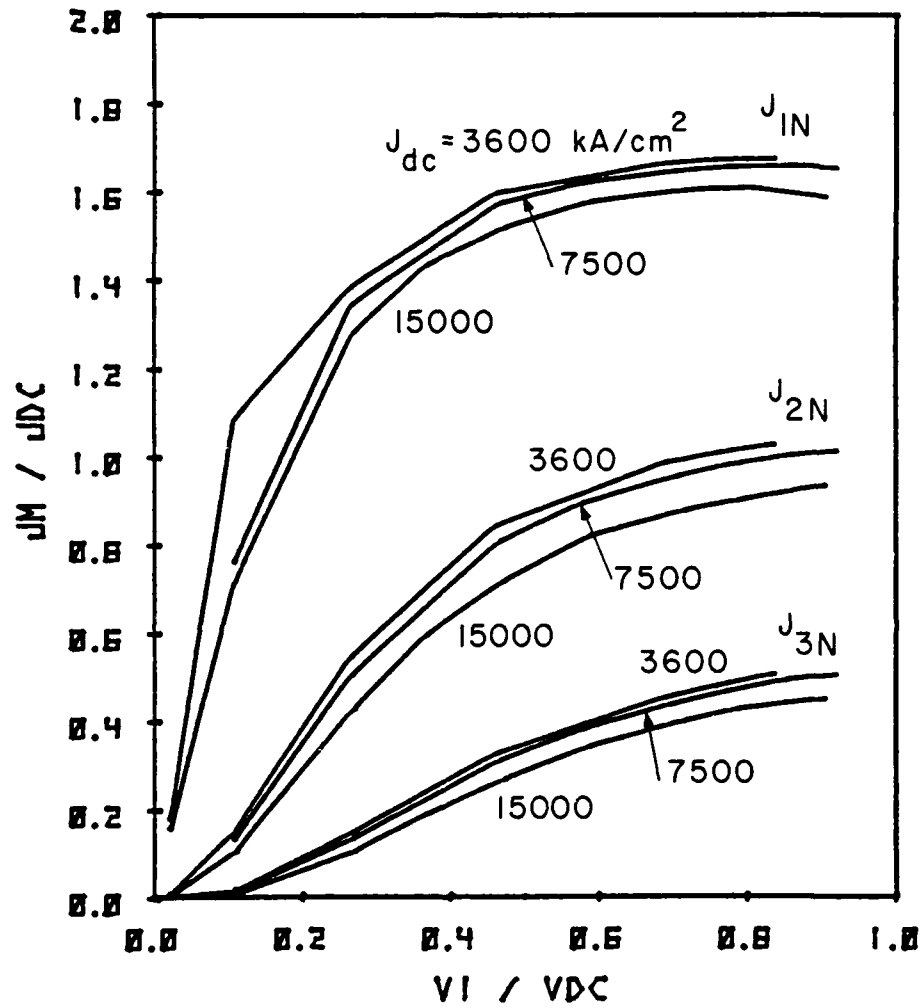
FIG. 2.50 NORMALIZED FUNDAMENTAL, SECOND- AND THIRD-HARMONIC
CURRENTS FOR pin DIODE 1 IN SINGLE-FREQUENCY
OPERATION.

at high dc current densities. This decrease is the consequence of
space-charge effects, as discussed previously, which will cause more
delay in the extraction of carriers and widen the induced current
waveform at high dc current densities. Despite this fact, the
normalized fundamental current can still become as high as 1.6.

The normalized harmonic current, also shown in Fig. 2.50,
does not rise as rapidly as the normalized fundamental current since
the induced current is not as sharp. It can be seen that the space-
charge effect also causes a decrease in the normalized harmonic current
at high dc current densities. The normalized second-harmonic current
can reach a maximum value of approximately 1.0 and the normalized
third-harmonic current can reach a maximum value of approximately
0.45. Both values are smaller than those achieved in the conventional
IMPATT diodes investigated before. It appears that in terms of har-
monic current generation, pin diode 1 is inferior in harmonic power
generation to the conventional IMPATT diode. However, the harmonic
current in pin diode 1 is less dependent on the driving RF voltage
than that in the conventional IMPATT diodes. This behavior permits
a high harmonic voltage to be applied to the diode together with a
fundamental voltage without degrading harmonic current too much.
Hence, high harmonic power generation can still be achieved in pin
diode 1. In addition, this diode has a low thermal resistance per
unit area due to short device length so the diode can be operated
at high dc current density.

The phase angle or phase delay of the Fourier components of
the induced current is another factor for understanding device per-
formance and this angle provides important information for determining

the required harmonic voltage to achieve the optimum harmonic power
generation. From Table 2.12 it is seen that the phase angles of the
fundamental and third-harmonic currents are decreasing as a functic
of terminal voltage and in contrast, that of the second-harmonic
current is an increasing function of terminal voltage. As pointed
out before, the phase angles of the harmonically related currents are
measured with reference to the fundamental voltage. If these are
plotted in a phasor plane, it would be found that these current phasors
rotate counterclockwise in the plane as the RF voltage increases.
Obviously increasing the RF voltage will increase charge densities
which, in turn, enhance the space-charge effect and turn off avalanche
multiplication in such a way that the induced current shifts to the
left. As a result, the phase delays of the currents relative to the
RF voltage are reduced. In other words, the current phasors rotate
counterclockwise in the phasor plane. It is interesting to note that
the phase delay of the fundamental current is close to 90 degrees.
This property implies that the negative fundamental device resistance
is very small except at high dc current densities.

The dc current density influences the phase angle in a very
complicated manner. At a given RF voltage, increasing the dc current
density will shift the induced current to the left and also increase
the induced current width. This produces counter effects on the phase
angle. The shift of the induced current has a dominant effect on the
phase angle of the third-harmonic current since this angle increases
with dc current density. However, variation of the phase angles of
the fundamental and second-harmonic currents with dc current density

is dependent on RF voltage. It is observed that the phase angle varies rapidly with RF voltage at high dc current densities.

The fundamental efficiency is determined from the behavior of the fundamental current and its phase angle. Figure 2.51 plots the fundamental efficiency as a function of normalized RF voltage. It can be observed from the figure that the fundamental efficiency is higher for lower dc current densities and saturates at high RF voltages. This saturation in the efficiency is related to the decrease of phase delay of the fundamental current at high RF voltages.

The dc voltage decreases with increasing RF voltage and this decreasing rate in dc voltage is higher at higher RF voltages. Except for the nonlinear ionization rates, the space-charge effect is another factor responsible for this behavior. The space-charge effect causes the electric field to swing nonuniformly in the depletion region. At higher RF voltages, the electric field in the central portion of the region has a more negative swing than a positive one. Therefore, the dc voltage must decrease more in order to balance the number of carriers generated and removed.

2.4.5b Performance of pin Diode 2. Pin diode 2 has a shorter device length than pin diode 1. The short device length of diode 2 implies a short transit time, which will result in a rapid collection of carriers generated in the depletion region, and a reduction in the space-charge effect. It is known that lowering the electric field in the central portion of the region is proportional to the amount of charge that remains in the region as well as the device length. Therefore, the lowering of the electric field in the central portion of pin diode 2 is not as great as that in pin
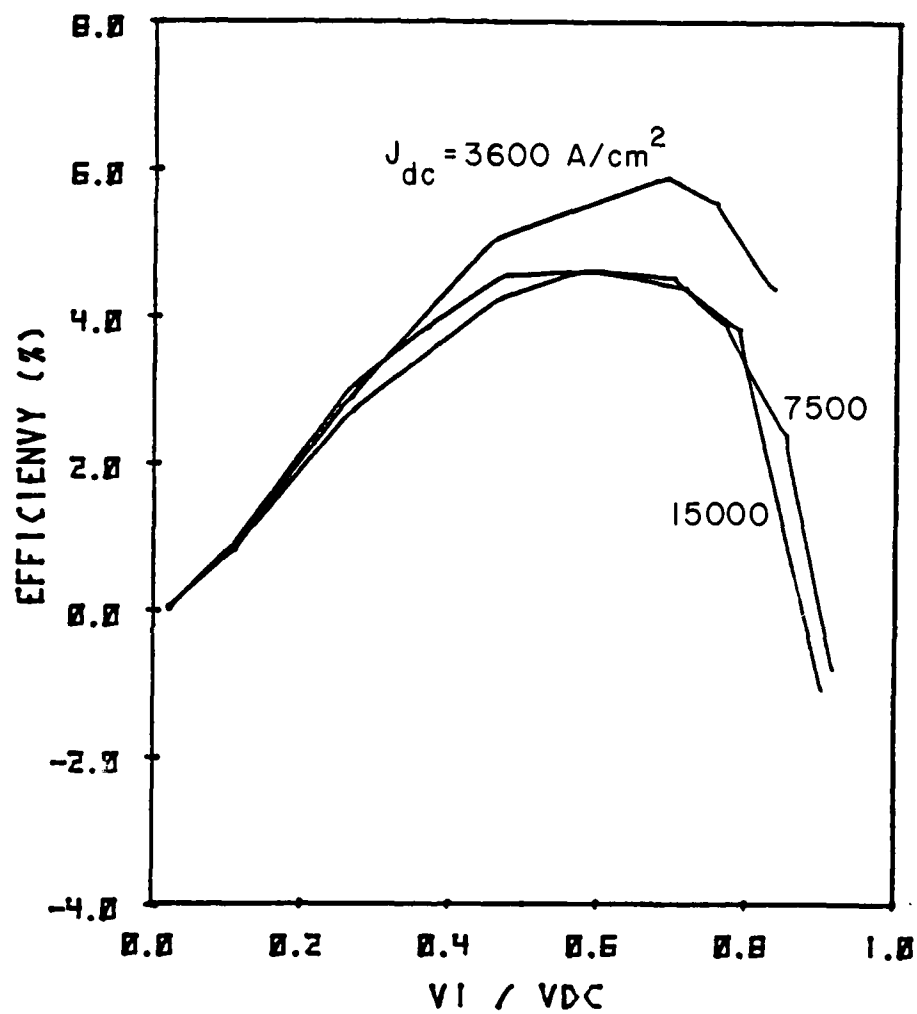
FIG. 2.51   FUNDAMENTAL EFFICIENCY AS A FUNCTION OF

NORMALIZED RF VOLTAGE FOR pin DIODE 1.

diode 1. As a result, the space-charge effect has less influence
on the performance of pin diode 2. This can be understood from Fig.
2.52, which shows the injected and induced current waveforms of this
diode at V_1 = 18 V. Some major characteristics of the injected
current are summarized in Table 2.13. From the data shown in the
table, the injected current peak position and width remain unchanged
when varying the dc current density, except that its peak magnitude
is slightly lower. By comparing this with that of pin diode 1, it
is seen that the injected current of pin diode 2 is sharper and
peaks later. Thus, the dc current density does not play a great role
in influencing avalanche multiplication. It is concluded that the
space-charge effect is not as significant as that in pin diode 1.

Table 2.13

Summary of Characteristics of the Injected Current

of pin Diode 2 at V_1 = 18 V

J_{dc} (kA/cm^2)	J_{injm} (kA/cm^2)	θ_p (Degrees)	θ_ω (Degrees)
3.6	31.6	151.2	39.6
7.5	64.4	151.2	39.6
15	124	151.2	39.6

The induced current at V_1 = 18 V has the characteristics
given in Table 2.14. By comparing these data with those of pin diode
1, it is seen that the induced current of pin diode 2 has a much sharper
and nearly symmetric waveform. The current peaks at the same instant
and increases slightly in the width while increasing dc current
density. In addition, the current drops almost to zero before the
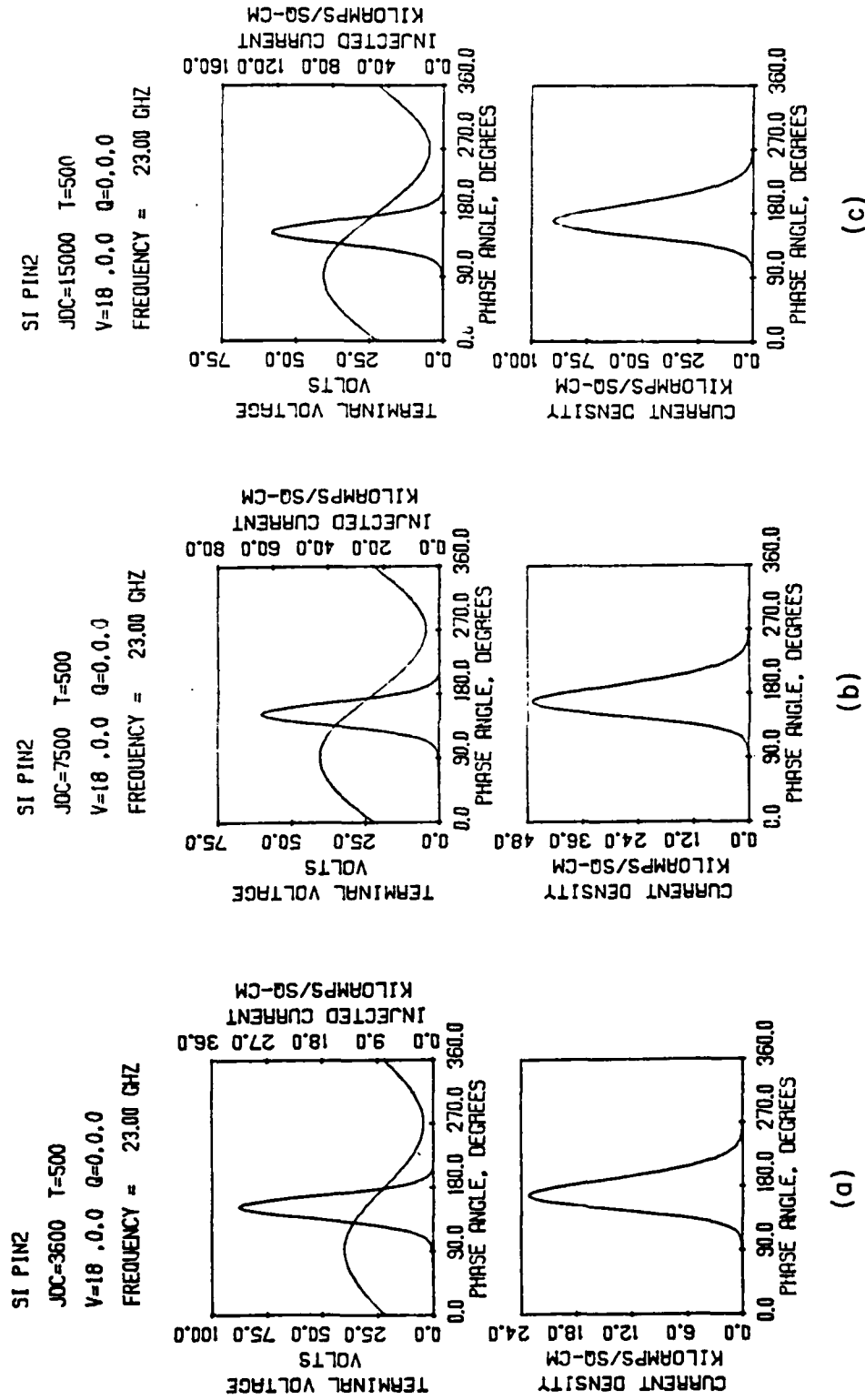
FIG. 2.52 LARGE-SIGNAL SOLUTIONS OF pin DIODE 2 AT V_1 = 18 V FOR THREE DIFFERENT dc CURRENT DENSITIES.

RF voltage reaches its minimum. This implies that velocity
modulation has a small effect on the current since most carriers
generated are collected before the electric field becomes low.
Therefore, increasing dc current density will not introduce a serious
space-charge effect in this diode.

Table 2.14

Summary of Characteristics of the Induced Current

of pin Diode 2 at V_1 = 18 V

J_{dc} (kA/cm^2)	J_{indm} (kA/cm^2)	θ_p (Degrees)	θ_L (Degrees)	θ_R (Degrees)	θ_ω (Degrees)
3.6	23.2	169.2	25.2	27	52.2
7.5	47.1	169.2	25.2	28.8	54
15	90.6	169.2	25.5	28.8	54

The large-signal results for pin diode 2 at various operating
conditions are listed in Table 2.15. The normalized fundamental
and harmonic currents are plotted in Fig. 2.53. Due to the sharp
induced current waveform in this diode, the normalized fundamental,
second- and third-harmonic currents can reach as high as 1.8, 1.4,
and 1.0, respectively. It is interesting to note that the normalized
third-harmonic current is more than twice that achieved in pin diode
1. Therefore, reduction in the device length of a pin diode can
significantly improve the device nonlinearity. As discussed previously,
the space-charge effect will not be enhanced with increasing dc
current density. Therefore, the normalized fundamental current only
decreases slightly at high dc current densities. Instead, the nor-
malized harmonic current drops much more, and this evidence indicates

Table 2.15

Large-Signal Results for pin Diode 2 in Single-Frequency Operation at Three Different Dc Current Densities

V_1			Eff (%)	P_1 (kW/cm^2)	J_1 (A/cm^2)	θ_{1I} (Deg.)	J_2 (A/cm^2)	θ_{2I} (Deg.)	J_3 (A/cm^2)	θ_{3I} (Deg.)
1.0	27.0	14955	0.04	0.1	7081	-92.3	822	68.5	148	-25.2
4.0	26.8	14705	1.09	4.3	20092	-96.1	7932	81.1	2055	-95.4
8.0	26.3	14615	1.75	6.7	24600	-93.9	14942	84.6	6796	-91.8
12.0	25.4	15.3	0.86	3.3	26749	-91.2	18846	89.6	10726	-85.4
16.0	23.7	14911	-3.19	-11.3	27181	-87.0	20549	97.7	13101	-74.0
19.0	21.8	14924	-9.76	-31.7	27411	-83.0	21356	105.7	14326	-62.4
1.0	27.0	7474	0.06	0.1	3681	-93.8	439	76.3	48	-46.2
4.0	26.9	7728	0.99	2.1	10744	-95.5	4425	82.2	1234	-94.3
3.0	26.4	7262	1.38	2.6	12338	-93.1	7709	86.1	3686	-90.5
12.0	25.5	7535	0.41	0.8	13434	-90.6	9717	90.6	5742	-84.8
16.0	23.7	7548	-4.24	-7.6	13817	-86.1	10638	99.3	6978	-72.4
19.0	21.6	7585	-11.76	-11.3	14007	-81.7	11088	108.0	7614	-59.6
1.0	27.2	3673	0.08	0.1	1838	-94.7	224	79.7	19	-70.8
4.0	27.1	3723	0.92	0.9	5226	-95.1	2201	82.7	639	-94.5
8.0	26.6	3491	1.29	1.2	5957	-92.9	3769	86.2	1838	-90.9
12.0	25.7	3495	0.34	0.3	6274	-90.5	4552	90.6	2732	-85.3
16.0	23.7	3607	-4.90	-4.2	6617	-85.5	5124	100.4	3388	-71.2
19.0	21.5	3605	-13.15	-10.2	6668	-80.7	5302	109.3	3662	-57.4
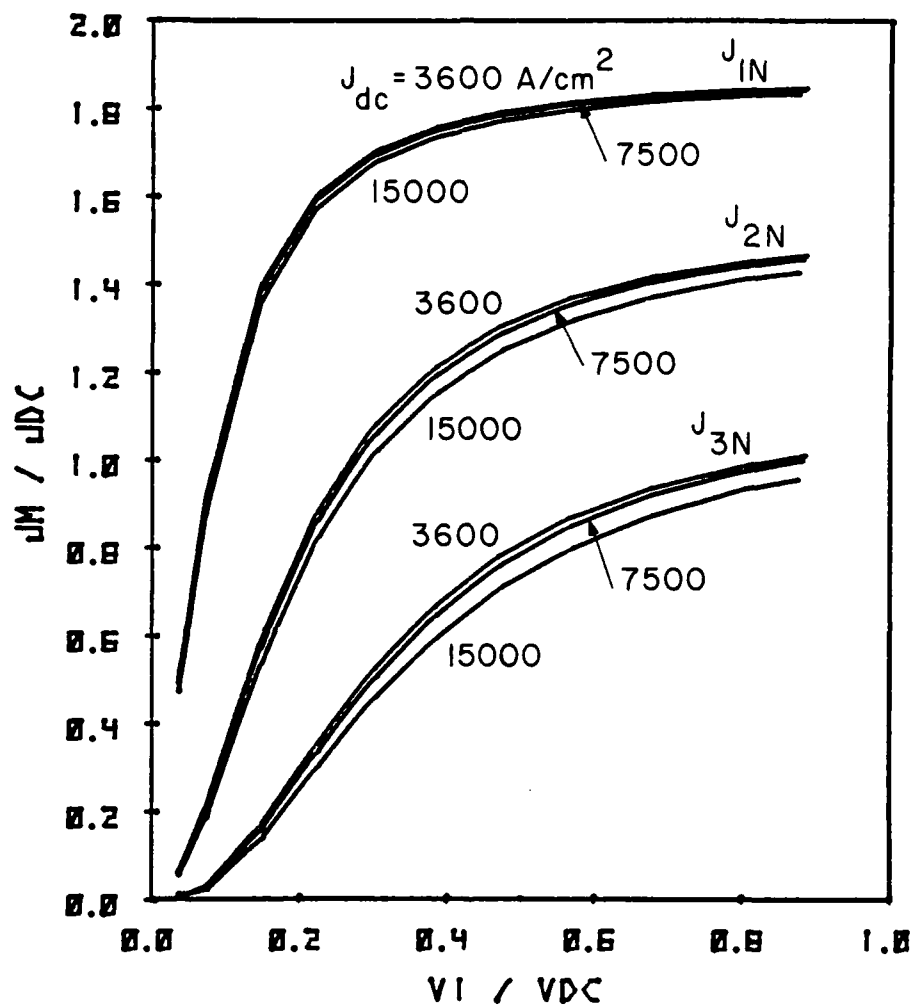
FIG. 2.53 NORMALIZED FUNDAMENTAL, SECOND- AND THIRD-HARMONIC

CURRENTS FOR pin DIODE 2 IN SINGLE-FREQUENCY

OPERATION.

that the space-charge effect induced by increasing dc current density still yields a certain influence on the harmonic current.

The behavior of the phase delay in this diode is different from that in pin diode 1 in several aspects. One is that the phase delay of the fundamental current is always less than that in diode 1, and the other is that the phase delay of each Fourier component increases at high dc current densities. Although the dc current has no significant effect on the avalanche multiplication, it still introduces great velocity modulation that delays the extraction of carriers. As a result, the induced current drops more slowly at high dc current densities and becomes more asymmetric in shape. According to Fourier analysis, the imaginary part of the fundamental current and the third-harmonic currents increases and that of the second-harmonic current decreases.

The fundamental efficiency is influenced by the behavior of the fundamental current phase delay in such a way that it becomes high at high dc current densities. Even so, the maximum efficiency achieved at $J_{dc} = 15$ kA/cm^2 is only 1.75 percent, which is much less than tha achieved in diode 1. Due to the sharpness of the induced current of diode 2, the phase delay of the fundamental current at low RF voltages is only a little greater than 90 degrees. As the RF voltage increases in magnitude, space charge is enhanced in a manner that the phase delay is reduced and is less than 90 degrees. As a consequence, the efficiency becomes negative at a relatively low RF voltage. This property is important for converting the fundamental power to the third harmonic in passive mode operation.

2.4.5c Performance of pin Diode 3. Pin diode 3 has a longer depletion region that can increase avalanche build-up time, delay the extraction of carriers generated in the depletion region, and enhance space-charge effects. In order to understand these effects on the injected and induced currents, the current waveforms at $V_1 =$ 40 V, which are shown in Fig. 2.54, are examined.

The injected current waveform becomes wider than those of the previous two diodes. Table 2.16 presents some information about the injected current shown in Fig. 2.54 for comparison.

Table 2.16

Summary of the Characteristics of the Injected Current

Waveform of pin Diode 3 at V_1 = 40 V

J_{dc} (kA/cm^2)	J_{injm} (kA/cm^2)	θ_p (Degrees)	θ_ω (Degrees)
3.6	24.9	144	50.4
7.5	49.7	140.4	50.4
15	88.3	136.8	54

In comparison with those of the other two diodes, the injected current in this diode is wider and has a small phase delay relative to the RF voltage (peaks close to 90 degrees) and has a low peak amplitude. Avalanche multiplication is not only seriously degraded but also prematurely turns off in this diode. The primary reason for this is due to the long device length, which results in significant lowering of the electric field in the depletion region. At high dc current densities, the lowering becomes more significant in reducing avalanche multiplication and the consequence is a reduction in the

-170-
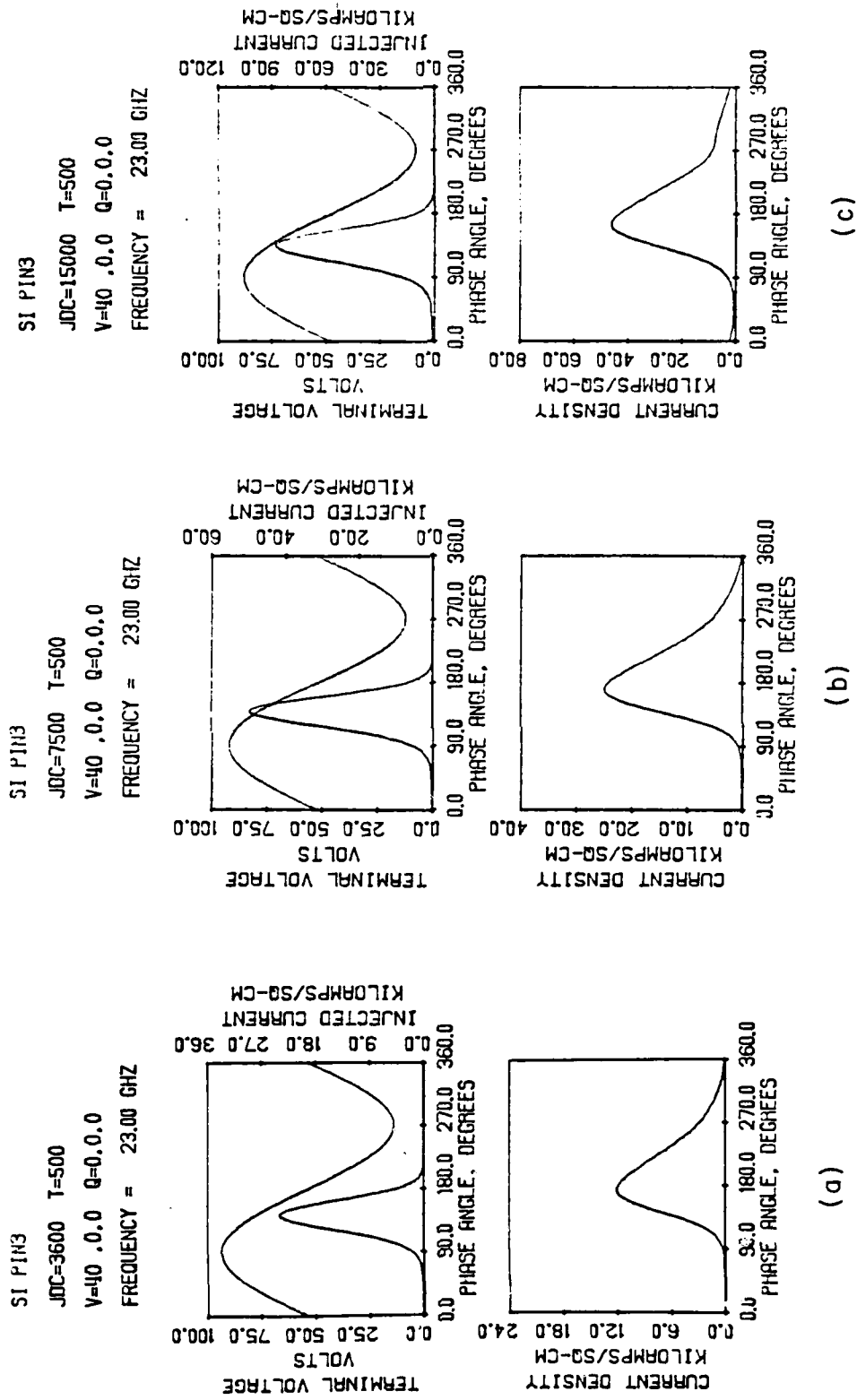
FIG. 2.54 LARGE-SIGNAL SOLUTIONS OF pin DIODE 3 AT V_1 = 40 V FOR THREE DIFFERENT dc CURRENT DENSITIES.
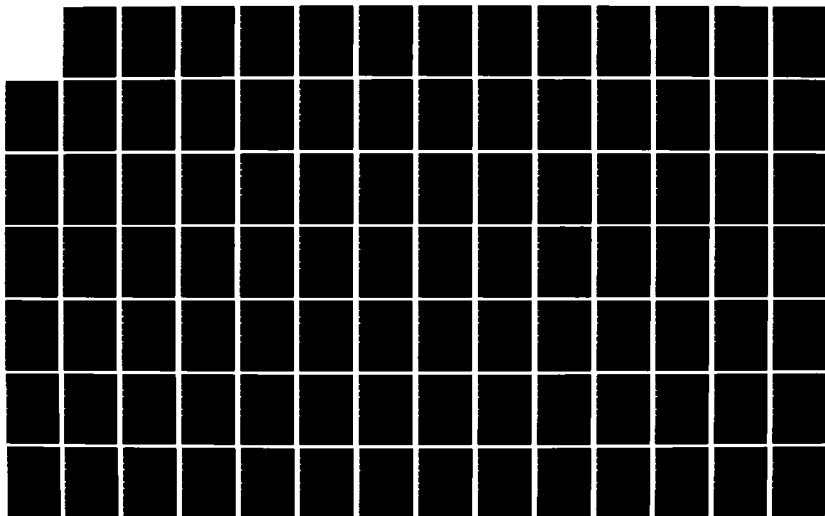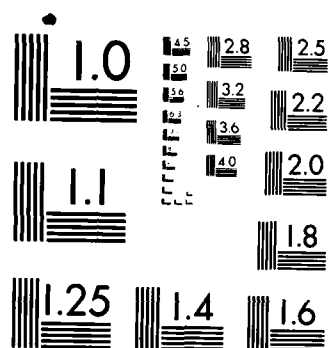
MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

phase delay of the injected current and an increase in the width of the current. The induced current has the characteristics given in Table 2.17.

Table 2.17

Summary of the Characteristics of the Induced Current

Waveform of pin Diode 3 at $V_1 = 40$ V

J_{dc} (kA/cm^2)	J_{indm} (kA/cm^2)	θ_p (Degrees)	θ_L (Degrees)	θ_R (Degrees)	θ_ω (Degrees)
3.6	12.3	175.5	36	64.8	100.8
7.5	24.8	170.9	36	64.8	100.8
15	46.2	166.4	36	61.2	97.2

From the data presented in Table 2.17 it is seen that the induced current is much wider than that of the other two diodes shown in Figs. 2.48 and 2.52 and its peak amplitude is also lower. It can be seen also from the table that the dc current density has a significant effect on the induced current as well as the injected current. The reason for causing the induced current to become wide is not only due to the injected current but also due to the long transit time. At $J_{dc} = 15$ kA/cm^2, the induced current seems to drop more rapidly than at low dc current densities. It is believed that the velocity modulation at $J_{dc} = 15$ kA/cm^2 is large enough to bring down the induced current. With this effect, the induced current is relatively higher at the RF voltage minimum and more carriers remain in the depletion-layer region. Hence, the induced current still flows at the beginning of the next RF cycle.

In order to examine the degradation in device nonlinearity due to the long device length, some large-signal results for this diode are listed in Table 2.18 and the normalized Fourier components of the induced current are plotted in Fig. 2.55. The normalized fundamental current rises slowly with increasing RF voltage and reaches a maximum in the range of 1.3, which is not much lower than that achieved in the other two diodes. Also the normalized fundamental current shows a strong dependence on dc current density. The normalized second-harmonic current, which also rises with RF voltage, can only achieve a maximum value of approximately 0.65. In addition, the normalized third-harmonic current reaches a maximum value of approximately 0.26 and shows a stronger dc current dependence than that in pin diode 1. It is concluded that the device nonlinearity is degraded by the long device length.

The phase angle provides additional information on the effect of long device length. From Table 2.16 it is seen that, except at low RF voltages, the phase delay of the fundamental current is relatively higher than in the other two diodes and is always in excess of 90 degrees. It is understandable that the slow fall off in the induced current due to long device length is the primary reason for this.

The fundamental efficiency is always positive and larger than that achieved in the other two diodes. In the voltage range of interest, the efficiency after reaching its maximum drops very rapidly with increasing RF voltage. It is also seen from the table that the corresponding dc voltage decreases in a similar way. At such high RF voltages the space-charge effect is very significant.

Table 2.18

Large-Signal Results for pin Diode 3 in Single-Frequency Operation at Three Different Dc Current Densities

V_1 (V)	V_{dc} (V)	J_{dc} (A/cm^2)	Eff (%)	P_1 (kW/cm^2)	J_1 (A/cm^2)	θ_{1I} (Deg.)	J_2 (A/cm^2)	θ_{2I} (Deg.)	J_3 (A/cm^2)	θ_{3I} (Deg.)
1.0	62.7	14627	0.01	0.1	1104	-93.3	62	14.2	41	-7.3
5.0	62.6	15269	0.43	4.1	5669	-106.7	537	93.1	38	-92.9
12.0	61.6	15387	2.05	19.4	12196	-105.4	2480	88.4	519	-56.2
20.0	59.6	14989	4.42	39.5	16448	-103.9	4691	88.2	1487	-54.8
30.0	56.0	14788	7.04	58.3	13860	-101.9	6626	92.1	2611	-52.6
36.0	53.2	14978	7.94	63.2	19667	-100.3	7690	96.9	3214	-52.2
40.0	48.5	15174	4.45	32.8	19307	-94.9	9446	107.8	3473	-51.4
1.0	63.4	7341	0.01	0.1	611	-101.9	22	30.1	12	-6.4
8.0	63.0	7535	1.05	5.0	4727	-105.3	702	82.9	97	-63.6
20.0	60.8	7545	4.82	22.1	8950	-104.3	2701	82.2	806	-52.9
30.0	57.7	7673	7.35	34.7	10416	-102.8	3864	84.5	1433	-60.8
38.0	53.8	7580	9.20	37.6	10677	-100.7	4436	89.3	1822	-58.1
40.0	52.3	7509	9.28	36.4	10585	-99.9	4603	92.3	1943	-53.8
42.0	48.2	7442	5.93	21.5	10163	-95.8	5089	101.5	2012	-59.6
1.0	63.4	7341	0.01	0.1	611	-101.9	22	30.1	12	-6.4
8.0	63.0	7535	1.05	5.0	4727	-105.3	702	32.9	97	-63.6
20.0	60.8	7545	4.82	22.1	8950	-104.3	2701	82.2	806	-62.9
30.0	57.7	7673	7.35	34.7	10416	-102.3	3864	84.5	1433	-60.8
38.0	53.8	7580	9.20	37.6	10677	-100.7	4436	89.3	1822	-58.1
40.0	52.3	7509	9.28	36.4	10585	-99.9	4603	92.3	1943	-53.8
42.0	48.2	7442	5.98	21.5	10163	-95.3	5089	101.5	2012	-59.6
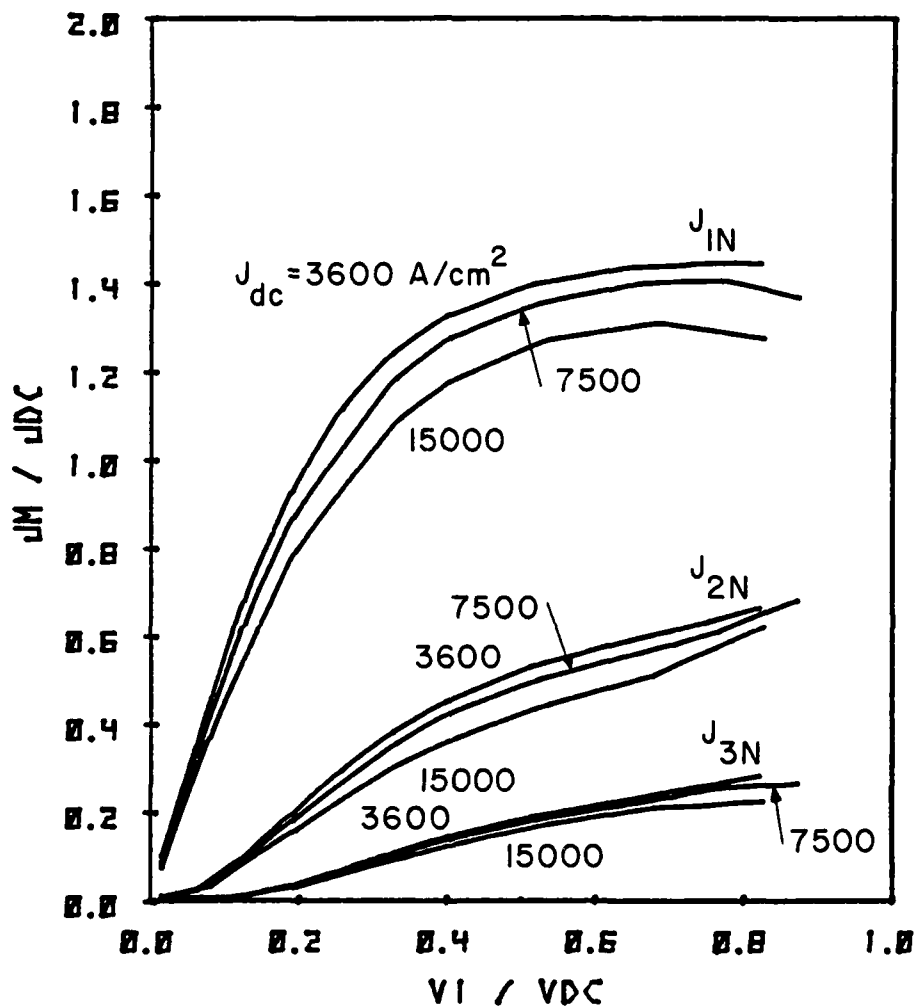
FIG. 2.55 NORMALIZED FUNDAMENTAL, SECOND- AND THIRD-HARMONIC

CURRENTS OF pin DIODE 3 IN SINGLE-FREQUENCY

OPERATION.

The electric field in the central portion is also greatly reduced during the interval between $\omega t = 180$ to 270 degrees. Consequently, the device performance is changed significantly by not only velocity modulation but also the back-bias effect.

2.4.5d Summary. Space-charge and transit-time effects, depending on device length, play essential roles in the device properties of pin diodes. Both effects are mutually related. For diodes having long device length, they may degrade the device nonlinearity but enhance the fundamental current phase delay. As a result, the fundamental efficiency of such diodes is high. For a diode having short device length, they will enhance device nonlinearity and cause the fundamental efficiency to become negative at relatively low RF voltages. This property guarantees that in such a short length diode, the passive mode of operation is easily achieved. Since the phase delay of the fundamental current of each pin diode investigated in close to 90 degrees, the magnitude of the device fundamental resistance is much less than that of the reactance. Increasing the dc current density can improve the device resistance level, but will introduce additional space-charge effects.

2.4.6 Multifrequency Operation of pin Diodes. In this section third-harmonic power generation in pin diodes in the passive mode of operation is considered. In order to operate diodes in this mode efficiently for frequency multiplication, the terminal voltage in the presence of a third-harmonic voltage must be optimized such that the diode can achieve high conversion efficiency (from fundamental power to third-harmonic power output) and also high device resistance levels for matching considerations (positive for the fundamental

resistance and negative for the third-harmonic resistance). In other words, the optimum terminal voltage must be able to reduce the phase delay of the induced current relative to the fundamental voltage such that the magnitude of the fundamental current phase angle is less than 90 degrees and also keep the phase difference between the third-harmonic voltage and current around 180 degrees. This condition can be achieved easily in a short-length pin diode, such as pin diode 2, that has a negative fundamental efficiency in single-frequency operation for relatively low RF voltages, but the negative resistance in the third harmonic is low in this short length diode. For a long pin diode, a high harmonic voltage is needed to convert the fundamental efficiency from positive to negative values. However, from the study in the previous section, it is seen that such a diode has a low harmonic·current that may not guarantee that the diode can achieve high third-harmonic resistance. Hence it is the purpose of this section to compare the performance of pin diodes with different lengths to determine the optimum device length at this particular fundamental frequency of 23 GHz for high third-harmonic power generation. Pin diode 1 is discussed in detail for understanding the effects of a third-harmonic voltage on the RF current components.

2.4.6a Third-Harmonic Power Generation in pin Diode 1.

In the presence of a third-harmonic voltage together with a fundamental voltage, the terminal voltage is not sinusoidal and will affect the induced current in a manner different from that in single-frequency operation. Basically the voltage waveform consists of two portions (positive and negative) with similar shapes. Unlike the

conventional IMPATT diode in which only the negative portion plays
an essential role in device performance, both portions play equally
important roles for the formation of the induced current. In general,
the positive one determines avalanche multiplication and the negative
one determines the extent of velocity modulation. By varying the
phase angle θ_{3V} of the third-harmonic voltage, the terminal voltage
peaks at different instants in the RF cycle as illustrated in Fig. 2.24.
For consideration of third-harmonic power generation it is worth
examining how the terminal voltage affects the injected and induced
currents and determining the optimum terminal voltage for high third-
harmonic current generation. According to these, the capability of
the pin diode for third-harmonic power generation in the passive mode
can be evaluated. The investigation is carried out for the case of
J_{dc} = 7.5 kA/cm^2.

Figure 2.56 illustrates the terminal voltage and injected and
induced current waveforms for V_1 = 28 V and V_3 = 8 V for four dif-
ferent values of θ_{3V}. The injected current is discussed first to
understand the influence of the terminal voltage on it. Table 2.19
summarizes some information about the injected current.

From the figure and table it is seen that the injected current
becomes sharper as θ_{3V} approaches 90 degrees and is degraded seriously
as θ_{3V} approaches 240 degrees. It seems that variation of the positive
portion of the RF voltage waveform is essential to affect the injected
current. At θ_{3V} = 0 degrees, the terminal RF voltage has two positive
peaks symmetrically appearing to the right and left sides of ωt =
90 degrees, respectively. As θ_{3V} increases from zero to 180 degrees,
the second peak (the right one) moves close to ωt = 90 degrees with an
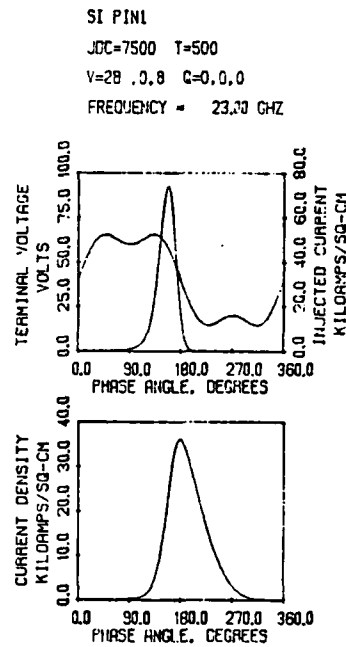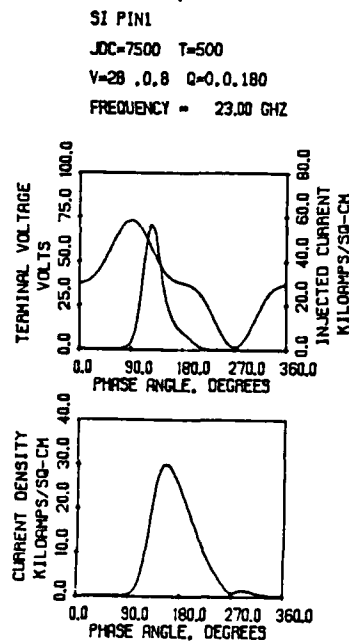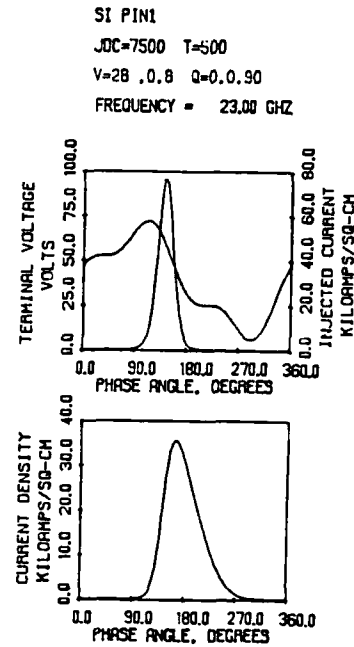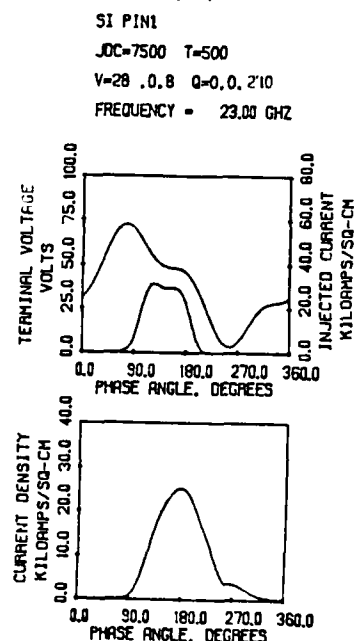
FIG. 2.56 LARGE-SIGNAL SOLUTIONS OF pin DIODE 1 AT

$J_{dc} = 7.5$ kA, $V_1 = 28$ V, AND $V_3 = 8$ V FOR

FOUR DIFFERENT θ_{3V}.

Table 2.19

Summary of Characteristics of the Injected Current of

pin Diode 1 at V_1 = 28 V, V_3 = 8 V, and J_{dc} = 7.5 kA/cm²

θ_{3V} (Degrees)	J_{injm} (kA/cm²)	θ_p (Degrees)	θ_ω (Degrees)
0	73.9	158.4	39.9
90	78.4	147.6	39.5
180	56.9	126	37.8
240	31.1	126	111.6

increase in magnitude, but the first one (the left one) gradually

disappears. As θ_{3V} decreases from 360 toward 180 degrees, the

first peak grows significantly and moves toward 90 degrees. At

θ_{3V} = 90 degrees, the RF voltage has only one positive peak.

According to Eq. 2.32, the injected current is a measure of the

charge generated in the depleted region so the injected current is

in proportion to the product of ionization rates and carrier densi-

ties in the region. The current becomes maximum when the product is

the highest. Usually, after ωt = 0 degrees, the carrier densities

build up through accumulation since most of the carriers generated

cannot be removed from the region, except those near the edges of the

depletion region. As long as the instantaneous terminal RF voltage

is positive, the increase in carrier densities continues until the

number of carriers removed from the depletion region is significant.

Therefore the carrier densities are highest at a certain instant

close to ωt = 180 degrees. Because the ionization rates are directly

proportional to the terminal voltage, the injected current is higher

if the terminal voltage peak is close to 180 degrees. The cases of θ_{3V} = 0 and 90 degrees fall into this category and hence the injected current peaks vary significantly. Between ωt = 90 and 180 degrees, the terminal voltage for θ_{3V} = 90 degrees has a higher positive peak value than that for θ_{3V} = 0 degrees and this makes the injected current at θ_{3V} = 90 degrees sharper. It is noted that the injected current usually peaks later than the voltage because of the properties of the carrier densities and ionization rates. Hence, increasing θ_{3V} moves the injected current to the left.

The injected current has a lower peak magnitude provided the voltage peaks far away from ωt = 180 degrees. The case of θ_{3V} = 180 and 240 degrees fall into this category. However, for θ_{3V} = 180 degrees, the voltage peak is highest than for any other case and the injected current can be still higher than that without applying the third-harmonic voltage. For θ_{3V} = 240 degrees, the main peak of the voltage appears at ωt = 75.6 degrees and at this moment the carrier density is not high enough to bring up the injected current. Beyond this moment, the voltage drops and keeps a small change over a certain range of ωt. Hence, the charge generation rate is limited by this lower terminal voltage and the carrier densities grow in a slow manner. As a consequence, the injected current is wide and low in magnitude.

The rise of the induced current is dependent upon whether the injected current is sharp or not, but the fall off in it is dependent on the transit time and velocity modulation of carriers. A summary of some characteristics of the induced current waveform is given in Table 2.20.

Table 2.20

Summary of Characteristics of the Induced Current of pin

Diode 1 at $V_1 = 28$ V, $V_3 = 8$ V, and $J_{dc} = 7.5$ kA/cm^3

θ_{3V} (Degrees)	J_{indm} (kA/cm^2)	θ_p (Degrees)	θ_L (Degrees)	θ_R (Degrees)	θ_ω (Degrees)
0	36.1	176.4	23.4	45	68.4
90	35.7	165.6	23.4	43.2	66.6
180	29.9	154.8	30.6	50.4	81
240	25.2	176.4	52.2	86.4	138.6

In comparison with that in the single-frequency operation shown in Fig. 2.48, an improvement in the induced current can be seen for the cases of $\theta_{3V} = 0$ and 90 degrees. The induced current at $\theta_{3V} = 90$ degrees rises as fast as that at $\theta_{3V} = 0$ degrees, but drops a little more quickly and reaches its peak early. This indicates that a proper third-harmonic voltage can improve the shape of the induced current and shift it to the left to make the fundamental efficiency negative.

The degradation in the induced current can be seen for the cases of $\theta_{3V} = 180$ and 240 degrees by a lowering in magnitude of the current peak and an increase in the width of the current. This degradation is clearly related to the slow growth of the carrier densities. Therefore, high harmonic current cannot be expected from such a poor induced current.

The variation of the phase delay (or phase angle) of the fundamental and third-harmonic currents is in proportion to the extent of the shift of the induced current waveform caused by the third-harmonic voltage. Obviously, the phase delay is reduced if

the induced current shifts to the left and is increased if the current shifts to the right. As a result the phase delay is minimum for θ_{3V} = 180 degrees and increases as θ_{3V} varies from 180 degrees. For instance, θ_{1I} = -80.3 degrees and θ_{3I} = -24.6 degrees for θ_{3V} = 180 degrees and θ_{1I} = -101.6 degrees and θ_{3I} = -100.7 degrees for θ_{3V} = 0 degrees. It is usually true that the phase delay of the third-harmonic current varies greatly with θ_{3V} compared with that of the fundamental current. Details about the effects of the third-harmonic voltage on the device performance can be understood from Fig. 2.57 which shows the current and efficiency for the fundamental and third harmonic at V_1 = 28 V. It can be seen from the figure that increasing V_3 will enhance the variation of the third-harmonic current amplitude. For θ_{3V} between -30 degrees (i.e., 330 degrees) and 120 degrees, the current is higher than that in the single-frequency operation at the same V_1 and increases with increasing V_3. This property, which is contrary to that for conventional IMPATT diodes, results from the improvement in the shape of the induced current waveform in the previously mentioned range of θ_{3V}. For θ_{3V} varying between 120 and 330 degrees, the third-harmonic current is a decreasing function of the third-harmonic voltage and becomes lowest at ωt = 240 degrees, where the induced current waveform has the worst shape.

The fundamental and third-harmonic efficiencies mainly depend on the behavior of the phase delays of the fundamental and third-harmonic currents, respectively. The behavior of the third-harmonic current phase delay, which decreases from θ_{3V} = 0 to 180 degrees and increases again beyond 180 degrees, yields a positive third-harmonic efficiency over a wide range of θ_{3V} extended from -30 to 240 degrees. Also, the third-harmonic efficiency is maximum at approximately θ_{3V} =
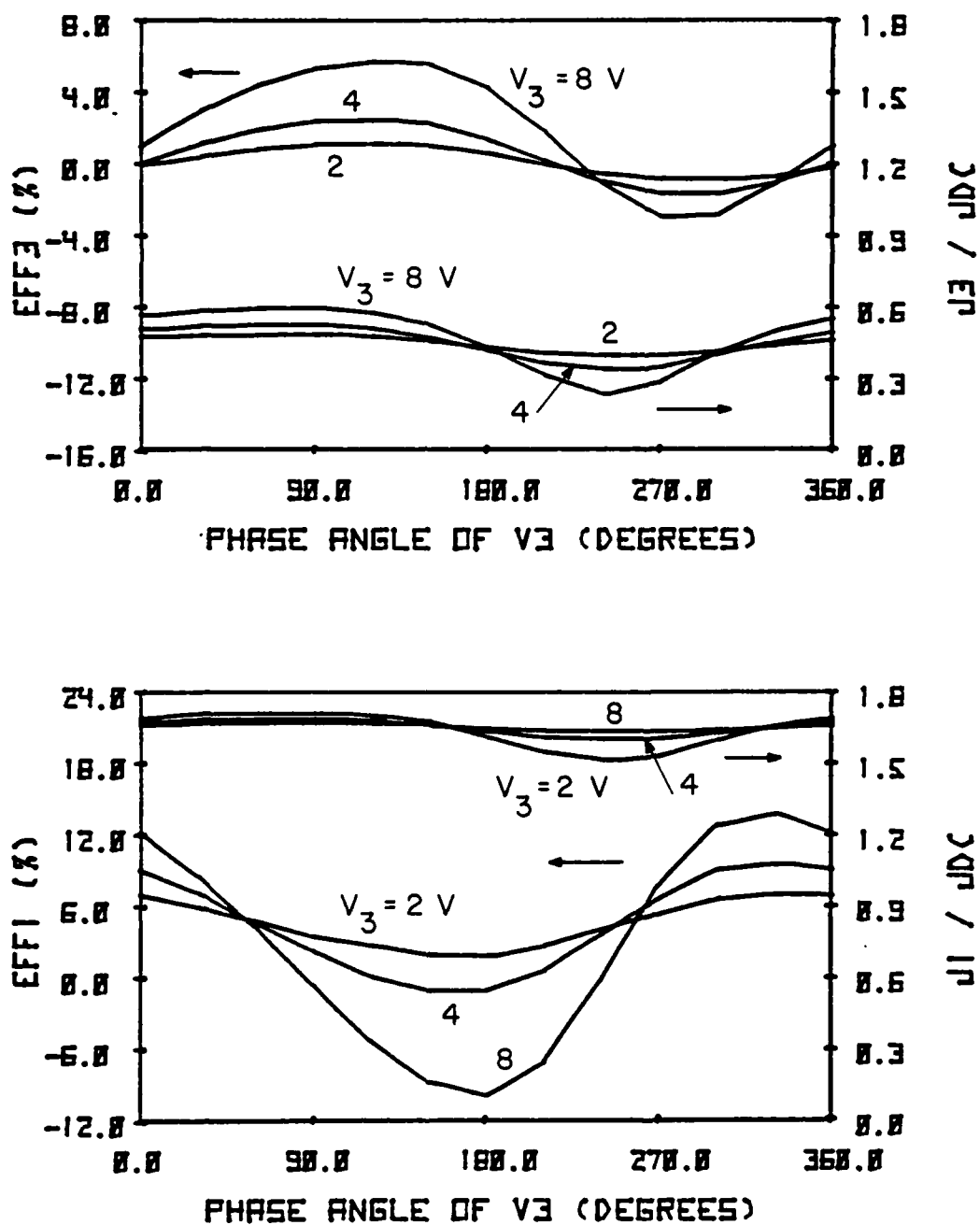
FIG. 2.57 FUNDAMENTAL AND THIRD-HARMONIC EFFICIENCIES AND

CURRENT DENSITIES AT J_{dc} = 7.5 kA/cm^2 AND

V_1 = 28 V.

120 degrees where the phase difference between the third-harmonic current and voltage is approximately 180 degrees. It is obvious that increasing V_3 can increase the maximum third-harmonic efficiency. For the fundamental, the efficiency at a given V_3 reaches its maximum at approximately $\theta_{3V} = 180$ degrees since the corresponding induced current has the largest shift to the left. Moreover, at this particular fundamental voltage, where the efficiency in single-frequency operation is positive, the efficiency at approximately $\theta_{3V} = 180$ degrees will gradually decrease and become negative for V_3 greater than 4 V. In other words, the required passive mode operation can be achieved only for V_3 greater than 4 V.

It is worth noting the behavior of the dc voltage under various third-harmonic voltages unlike that in conventional IMPATT diodes, the dc voltage undergoes a small change with V_3 and θ_{3V}. For example, at $\theta_{3V} = 0$ degrees, $V_{dc} = 40.223$ V for $V_3 = 2$ V and $V_{dc} = 39.993$ V for $V_3 = 8$ V. At $\theta_{3V} = 180$ degrees, $V_{dc} = 39.656$ V for $V_3 = 2$ V and $V_{dc} = 37.34$ V for $V_3 = 8$ V compared with $V_{dc} = 40.048$ V for $V_3 = 0$ V. The third-harmonic voltage produces little effect on the dc voltage. This behavior in dc voltage restrains the maximum amplitude of V_3 which can be applied to the terminal, particularly for high values of V_1. For further simulation, the maximum V_3 is kept less than $V_{dc} - V_1$.

In order to evaluate the capability of the pin diodes for frequency multiplication it is necessary to look at the third-harmonic power density that can be obtained from simulation and the conversion efficiency Eff_{13} which is defined as

$$Eff_{13} = -\frac{Eff_3}{Eff_1} = -\frac{P_3}{P_1} . \tag{2.64}$$

According to this definition, the conversion efficiency clearly is a function of V_1, V_3 and θ_{3V}. It is possible for some situations that Eff_1 be zero so that the conversion efficiency becomes infinite. Although the infinite conversion efficiency means that no fundamental power is needed to generate third-harmonic power, there is no guarantee that for such a situation the corresponding third-harmonic power output is maximum. Since fundamental power is readily available, it is better to evaluate the conversion efficiency at the points near the maximum third-harmonic power output points. However, the corresponding fundamental resistance is not usually maximum (it is maximized at θ_{3V} = 180 degrees) so that the conversion efficiency can be degraded by the series resistance. To evaluate the effect of series resistance, an equivalent circuit for pin diodes in the passive mode, which is shown in Fig. 2.58, is considered.

Because of the sign convention adopted, the input fundamental power P_1 is treated as negative, but the third-harmonic power output is treated as positive. Including the series resistance, the conversion efficiency Eff'_{13} can be expressed as

$$Eff'_{13} = -\frac{P'_3}{P'_1} = -\frac{P_3 \dfrac{|R_{d3}| - R_s}{|R_{d3}|}}{P_1 \dfrac{R_s + R_{d1}}{R_{d1}}}$$

$$= Eff_{13} \frac{1 - \dfrac{R_s}{|R_{d3}|}}{1 + \dfrac{R_s}{R_{d1}}} , \qquad (2.65)$$

where Eff_{13} is the conversion efficiency without taking into account the series resistance. Rearranging the preceding equation and
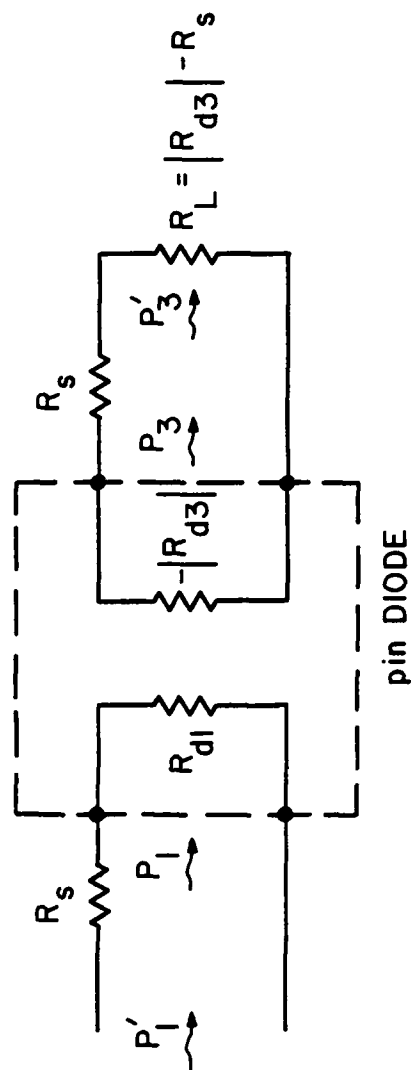
FIG. 2.58 AN EQUIVALENT CIRCUIT FOR A pin DIODE IN THE PASSIVE MODE.

assuming R_s/R_{d1} is very small yields

$$Eff'_{13} = Eff_{13}\left(1 - \frac{R_s}{R_{d1}}\right)(1 - R_s/|R_{d3}|) = Eff_{13}\left[1 - \left(\frac{R_s}{|R_{d3}|} + \frac{R_s}{R_{d1}}\right)\right]$$

$$+ \frac{R_s^2}{R_{d1}|R_{d3}|}\right] = Eff_{13}\left(1 - \frac{R_s}{R_{d1}||\,|R_{d3}|} + \frac{R_s^2}{R_{d1}|R_{d3}|}\right) \quad . \quad (2.66)$$

The last term in parentheses of Eq. 2.66 is small compared with the other two terms and can be neglected. Minimizing the degradation in conversion efficiency caused by the series resistance demands that $R_{d1} || |R_{d3}|$ should be as large as possible. Hence, through-out this section the conversion efficiency for a given V_1 and V_3 is evaluated at the phase angle θ_{3V} such that the corresponding $R_{d1} || |R_{d3}|$ is maximum. (Fortunately, the corresponding third-harmonic power is close to the maximum value.) This can also avoid the occurrence of infinite conversion efficiency. Based on such criteria, the per-formance of pin diode 1 at various operating conditions is presented in Figs. 2.59 to 2.61.

The third-harmonic power density is plotted in Fig. 2.59. It is apparent from the figure that increasing dc current density enhances the third-harmonic power output. Since the thermal effect is not serious it is better to operate the diode at high dc current density. An interesting aspect from this figure is that for a given J_{dc} the rate of change of the third-harmonic power relative to the third-harmonic voltage is almost the same for different fundamental voltages. The primary reason is due to the fact that for the cases considered, θ_{3V} is approximately 120 degrees and the third-harmonic current is only enhanced a little while increasing the
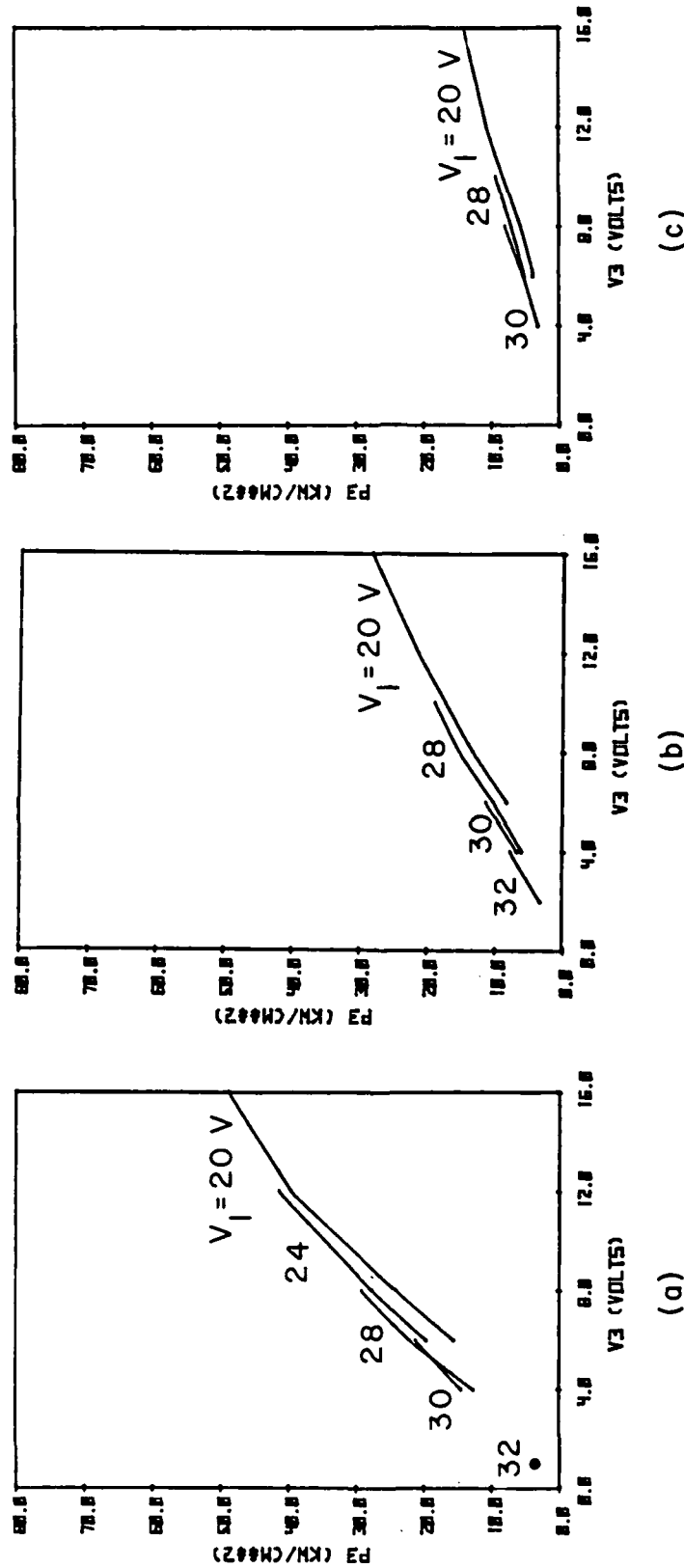
FIG. 2.59 THIRD-HARMONIC POWER DENSITY ACHIEVED IN pin DIODE 1 AT VARIOUS OPERATING CONDITIONS.

(a) J_{dc} = 15 kA/cm^2, (b) J_{dc} = 7.5 kA/cm^2 AND (c) J_{dc} = 3.6 kA/cm^2.
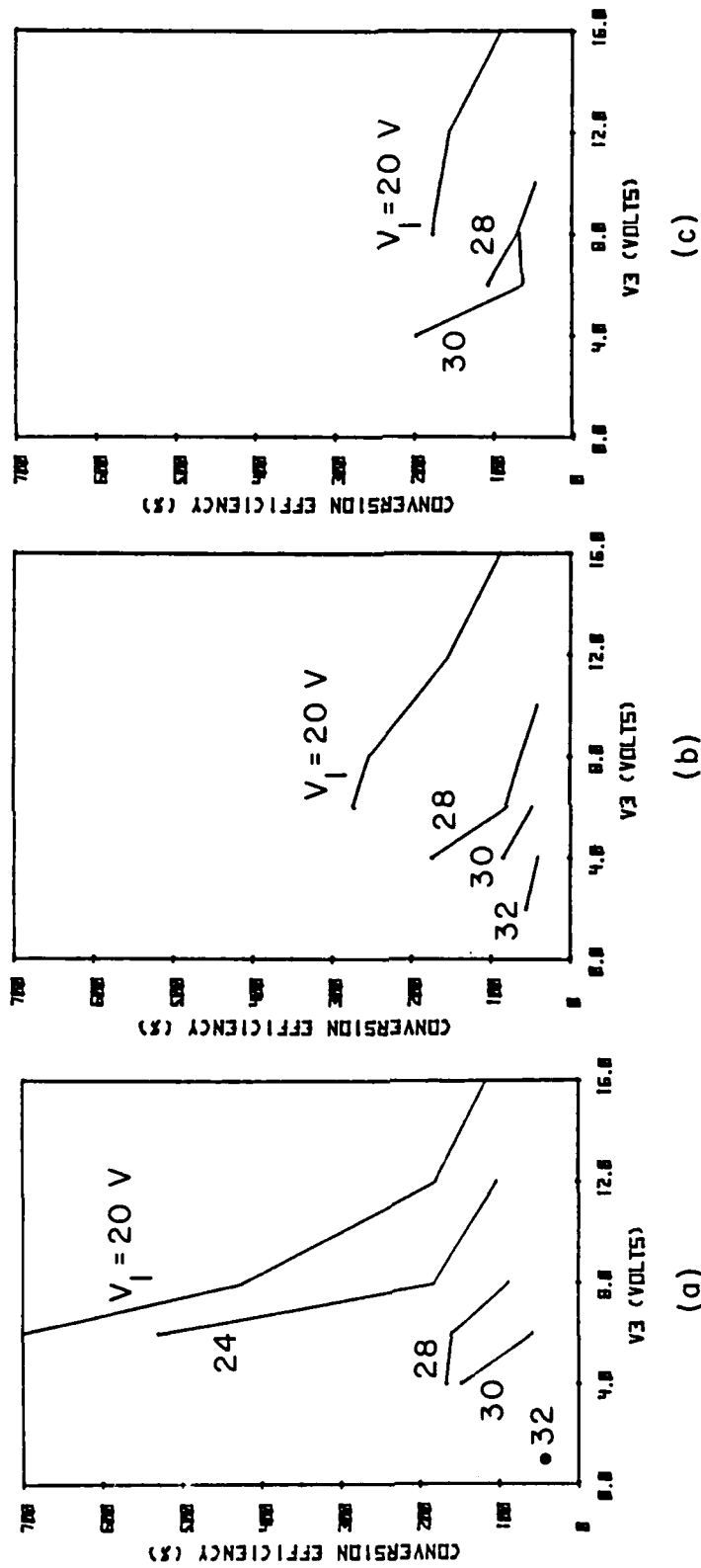
FIG. 2.60 CONVERSION EFFICIENCY ACHIEVED IN pin DIODE 1 AT VARIOUS CONDITIONS.

(a) $J_{dc} = 15$ kA/cm^2, (b) $J_{dc} = 7.5$ kA/cm^2 AND (c) $J_{dc} = 3.6$ kA/cm^2.
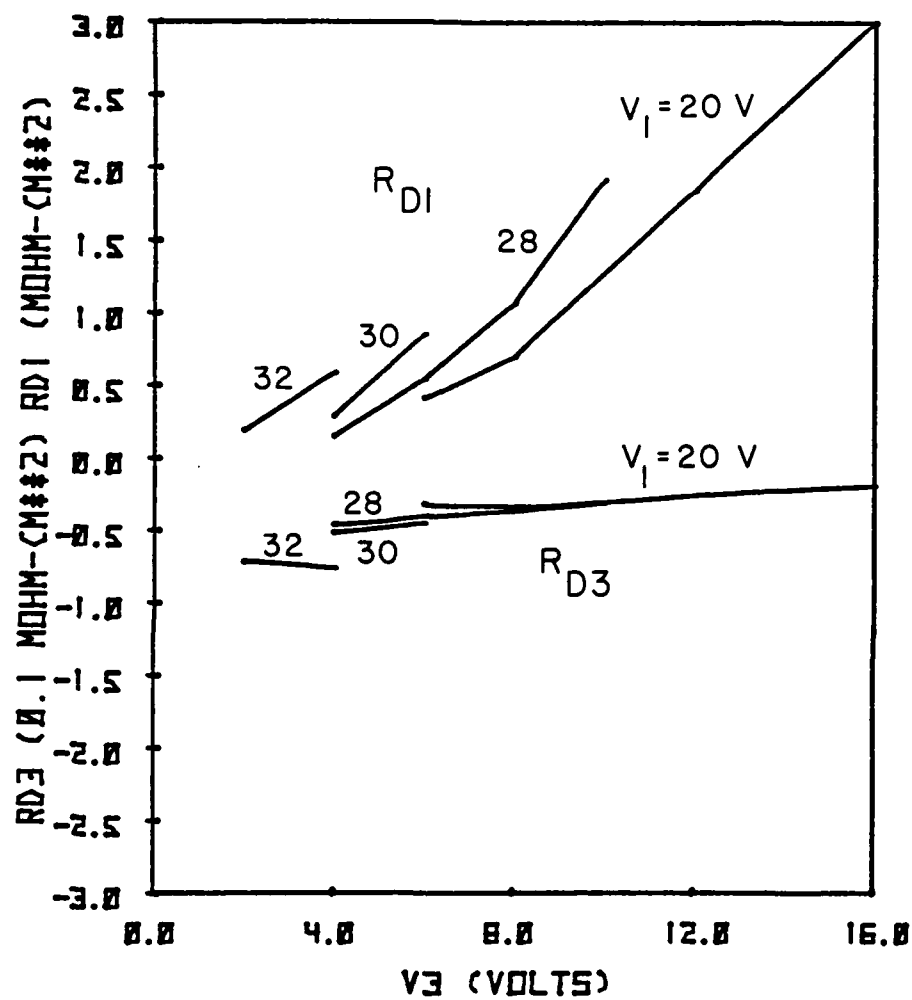
FIG. 2.61   FUNDAMENTAL AND THIRD-HARMONIC RESISTANCE OF

pin DIODE 1 AT J_{dc} = 7.5 kA/cm^2.

third-harmonic voltage. Hence, the third-harmonic output is almost
linearly dependent on the third-harmonic voltage. The conversion
efficiency as a function of V_3 is plotted in Fig. 2.60. As shown
in this figure, the conversion efficiency for a given V_1 is a de-
creasing function of V_3; at some points the efficiency can be higher
than 100 percent. However, combining Figs. 2.59 and 2.60 shows that
for any given V_1 the third-harmonic power output is not the highest
at the maximum conversion efficiency points. This reflects a fact
that the conversion efficiency is not the best way to compare the
device capability for frequency multiplication. As is known from
the single-frequency operation, this diode has a positive efficiency
until V_1 is extremely high. Therefore, for most V_1, a not too low
third-harmonic voltage is needed in order to convert the fundamental
efficiency from positive to negative values. There may be a third-
harmonic voltage at which the fundamental efficiency exhibits a small
negative value for certain θ_{3V}. At such conditions, the corres-
ponding conversion efficiency is very high. As V_1 continues to
increase, the fundamental efficiency becomes more negative, and this
brings down the conversion efficiency. It is also learned from
single-frequency operation that at low fundamental voltages the
fundamental current has a large phase delay due to the small space-
charge effect. Similarly, for a given V_3 in multifrequency operation,
a low fundamental voltage only introduces a small space-charge
effect, which in turn increases the phase delay of the fundamental
current slightly. Hence the conversion efficiency is high for low
fundamental voltages.

The device resistance also plays an essential role in the evaluation of third-harmonic power output. In proportion to device conductance, the device resistance at either the fundamental or third harmonic depends on the ratio $J_m/V_m \cos(\theta_{mV} - \theta_{mI})$. For the data points shown in Fig. 2.59, the corresponding phase difference $\theta_{3V} - \theta_3$ is always in the range from 150 to 200 degrees, but the third-harmonic current does not exhibit too much variation in magnitude. For example, for $J_{dc} = 7.5$ kA/cm^2, the corresponding J_3 varies between 3 and 4 kA/cm^2. Therefore, the third-harmonic resistance is nearly inversely proportional to the third-harmonic voltage. The corresponding fundamental current for the same data points, which is more stable than the corresponding third-harmonic current, has only a few percent variation, but the phase difference $\theta_{1V} - \theta_{1I}$, which is always less than 90 degrees, decreases while increasing the third-harmonic voltage. Therefore, for a given fundamental voltage, the ratio J_1/V_1 remains almost unchanged, but the value of $\cos(\theta_{1V} - \theta_{1I})$ is an increasing function of V_3. This results in the increasing behavior of the fundamental resistance with V_3. A typical example is illustrated in Fig. 2.61 which shows the corresponding resistance for the fundamental and third harmonic for the data points shown in Fig. 2.59 at $J_{dc} = 7.5$ kA/cm^2. From this figure, with increasing V_3, the fundamental resistance indeed increases in magnitude, and the third-harmonic resistance linearly decreases in magnitude except for the case of $V_1 = 32$ V where convergent solutions may not be obtained as θ_{3V} is greater than 120 degrees. It can be seen from the figure that the magnitude of the third-harmonic resistance for this particular dc current density

is less than 10^{-4} Ω-cm^2. Although a high dc current density can enhance the magnitude of the third-harmonic resistance, the property that the magnitude decreases with V_3 makes it impossible to operate pin diode 1 at high V_3 where high third-harmonic power is expected.

At first the third-harmonic power output is calculated by considering only circuit-matching effects. The diode area is chosen such that the magnitude of device resistance (not per unit area) at the fundamental and third harmonic is greater than or equal to 1 Ω. The best way to achieve this is to make the device area equal to the minimum value between the magnitudes of both resistances in per unit area. On the basis of this principle, the maximum third-harmonic power output for each J_{dc} and V_1 is calculated and presented in Table 2.21.

One of several interesting aspects from the results of this table is that the maximum third-harmonic power for a given J_{dc} is almost independent of the operating fundamental voltage. This can be understood from the behavior of the magnitude and phase angle of the third-harmonic current since the power output P_{3out} is calculated by the following formula:

$$P_{3out} = \frac{1}{2} V_3^2 |G_{d3}| \frac{|G_{d3}|}{G_{d3}^2 + B_{d3}^2} , \qquad (2.67)$$

where $G_{d3} = (J_3/V_3) \cos(\theta_{3V} - \theta_{3I})$. Substituting G_{d3} into Eq. 2.67 yields

$$P_{3out} = \frac{1}{2} J_{dc}^2 \frac{J_{3N}^2}{G_{d3}^2 + B_{d3}^2} \cos^2(\theta_{3V} - \theta_{3I}) . \qquad (2.68)$$

For most cases considered, $B_{d3}^2 >> G_{d3}^2$ and $-\cos(\theta_{3V} - \theta_{3I})$ is close

Table 2.21

Power Output for pin Diode 1 Taking into Account Circuit Matching Only

V_1 (V)	V_3 (V)	J_{dc} (kA/cm²)	R_{d1} (Ω)	R_{d3} (Ω)	A (10^{-4}, cm²)	V_{dc} (V)	Eff (%)³	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
32.0	1.0	15.1	1.0	-1.5	0.81	35.65	41.42	43.6	0.283	4.0	4.6
30.0	6.0	14.6	4.7	-1.0	1.00	35.68	58.37	52.0	2.126	4.4	3.8
28.0	8.0	14.7	8.7	-1.0	0.79	37.07	88.27	42.9	2.295	3.9	4.7
24.0	12.0	14.9	38.4	-1.0	0.52	37.66	102.56	28.4	2.143	3.2	7.1
20.0	12.0	15.3	177.3	-1.0	0.50	39.86	179.81	30.6	1.979	3.1	6.8
33.0	2.0	7.3	1.0	-12.2	0.14	35.79	65.43	3.6	0.048	1.7	55.1
32.0	4.0	7.5	1.0	-1.3	0.59	35.16	39.48	21.5	0.468	3.4	9.0
30.0	6.0	7.6	1.9	-1.0	0.45	36.79	48.24	12.5	0.512	3.0	15.5
28.0	10.0	7.5	6.4	-1.0	0.30	34.52	40.69	7.7	0.572	2.4	23.6
24.0	12.0	7.7	8.4	-1.0	0.26	33.28	75.27	7.7	0.624	2.3	25.4
32.0	4.0	3.7	1.0	-5.3	0.07	37.16	106.74	1.0	0.029	1.2	198.1
30.0	8.0	3.6	1.3	-1.0	0.20	36.07	68.21	2.6	0.165	2.0	75.6
28.0	10.0	3.5	3.6	-1.0	0.14	35.37	45.92	1.8	0.136	1.7	103.3
24.0	12.0	3.6	3.4	-1.0	0.12	38.76	106.46	1.7	0.143	1.6	116.5

to one and J_{3N} does not vary greatly at different optimum operational terminal voltages. Consequently, the third-harmonic power output for a given dc current density is not dependent on the fundamental voltage, provided that the space-charge effect is not too serious. The other interesting aspect is that the maximum third-harmonic power for a given V_1 is quadratically proportional to the dc current density. According to the same reason given before, the quadratic dependence can be expected from Eq. 2.68.

From Table 2.21, the maximum conversion efficiency achieved for pin diode 1 is 102 percent for J_{dc} = 15 kA/cm^2 and V_1 = 24 V. The maximum third-harmonic power output is 2.295 W at J_{dc} = 15 kA/cm^2 and V_1 = 28 V.

In order to evaluate the third-harmonic power output including the thermal constraint, the same procedure used for the conventional IMPATT is adopted where diode t_2 in Eq. 2.51 is taken to be equal to the device length of pin diode 1 (1.2 μm) and the maximum device temperature is still assumed to be 500°K. The calculation is carried out for four different types of heat sink structures, and only the results for maximum third-harmonic power output for different dc current densities and heat sink structures are listed in Table 2.22. It can be observed from the table that (1) at low dc current density, such as 3.6 kA/cm^2, the thermal effect does not impose a constraint on the output power; (2) at medium dc current density, such as 7.5 kA/cm^2, the thermal effect only constrains the output power from the single mesa structure on a copper heat sink; and (3) at a high dc current density, such as 15 kA/cm^2, the thermal effects plays an essential role in the capability of the third-harmonic power

Table 2.22

CW Power Output for pin Diode 1 Taking into Account Thermal Limitations

J_{dc} (kA/cm²)		V_1 (V)	V_3 (V)	θ_{3V} (Deg.)	I_{dc} (A)	P_{dc} (W)	V_{dc} (V)	Eff_{13} (%)	R_{d1} (Ω)	R_{d3} (Ω)	P_3 (W)	D (mils)	R_{th} (°C/W)
15	- CM	20.0	16.0	120.0	0.03	1.20	37.29	115.97	2008.96	-16.09	0.106	0.7	170.0
7.5	- CM	20.0	16.0	150.0	0.11	4.02	37.81	87.97	26.02	-1.28	0.400	1.7	49.6
3.6	- CM	30.0	8.0	120.0	0.07	2.60	36.07	68.21	1.31	-1.00	0.165	2.0	40.0
15	- DM	20.0	16.0	120.0	0.29	10.83	37.29	115.97	223.15	-1.79	0.957	2.0	18.9
7.5	- DM	24.0	12.0	150.0	0.20	7.74	38.28	75.27	8.41	-1.00	0.624	2.3	15.4
3.6	- DM	30.0	8.0	120.0	0.07	2.60	36.07	68.21	1.31	-1.00	0.165	2.0	18.5
15	- CR	20.0	16.0	120.0	0.11	3.98	37.29	115.97	607.76	-4.87	0.351	1.2	51.4
7.5	- CR	24.0	12.0	150.0	0.20	7.74	38.28	75.27	8.41	-1.00	0.624	2.3	21.5
3.6	- CR	30.0	8.0	120.0	0.07	2.60	36.07	68.21	1.31	-1.00	0.165	2.0	25.5
15	- DR	24.0	12.0	120.0	0.77	23.45	37.66	102.56	38.43	-1.00	2.143	3.2	6.7
7.5	- DR	24.0	12.0	150.0	0.20	7.74	38.28	75.27	8.41	-1.00	0.624	2.3	11.1
3.6	- DR	30.0	8.0	120.0	0.07	2.60	36.07	68.21	1.31	-1.00	0.165	2.0	13.7

generation of pin diode 1. The single mesa on a copper heat sink structure gives the lowest power output and the ring geometry on a diamond heat sink gives the highest power output, which is still less than the maximum value achieved by considering only the circuit-matching effect.

2.4.6b   Third-Harmonic Power Generation in pin Diode 2.

Pin diode 2 has a shorter device length than pin diode 1. In single-frequency operation, its short device length yields a much different performance from that of pin diode 1. In multifrequency operation, it is interesting to compare the performance difference between them and to see whether reducing device length can improve the capability for converting the fundamental power to the third-harmonic power. In the following, the performance of pin diode 2 at $V_1 = 16$ V and $J_{dc} = 7.5$ kA/cm^2 is discussed first.

Figure 2.62 shows the properties of pin diode 2 at $V_1 = 16$ V and $J_{dc} = 7.5$ kA/cm^2. This diode has a voltage modulation ratio of 0.676 at $V_3 = 0$ V, which is close to the value of 0.699 for the case of pin diode 1 shown in Fig. 2.57. The third-harmonic voltage applied to pin diode 2 is one half of that indicated in Fig. 2.57. It can be seen in Fig. 2.62 that the normalized fundamental current does not exhibit a significant change while increasing V_3, except at $V_1 = 4$ V and $\theta_{3V} = 240$ degrees where the current drops a little. The normalized fundamental current is close to the ideal limit, two, due to the sharp induced current waveform. Any reduction in the induced current width may not cause the normalized fundamental current to increase significantly. The normalized third-harmonic current does show a certain variation with V_3. The maximum achievable magnitude
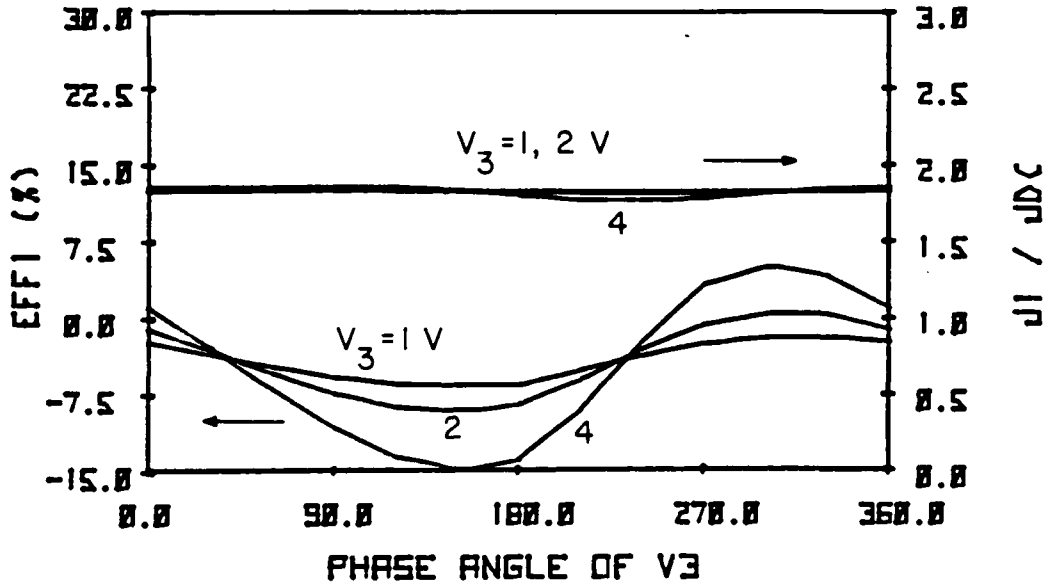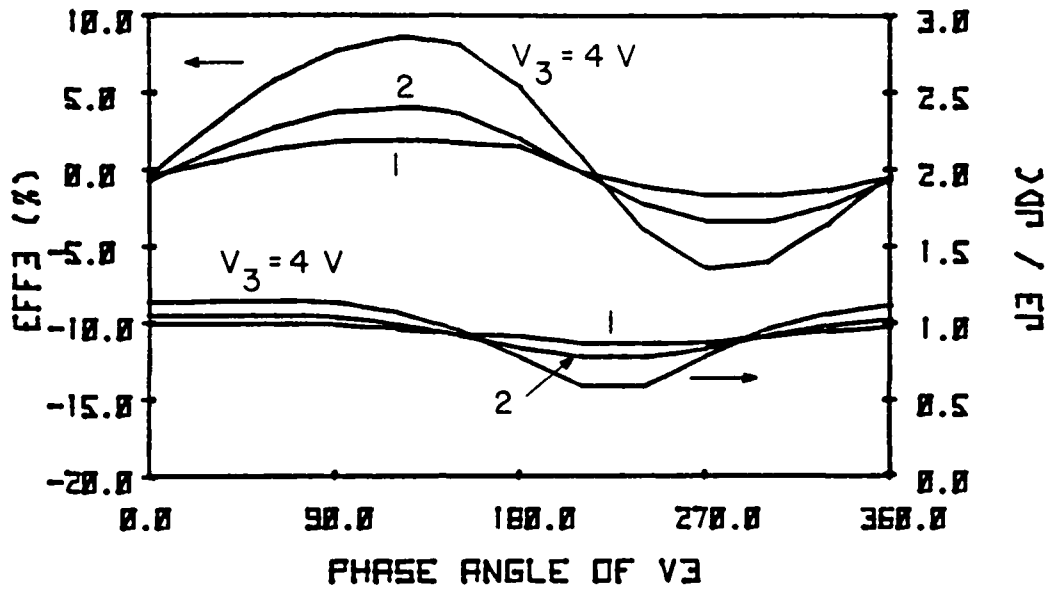
FIG. 2.62 FUNDAMENTAL AND THIRD-HARMONIC EFFICIENCIES AND

CURRENTS FOR pin DIODE 2 AT J_{dc} = 7.5 kA/cm^2 AND

V_1 = 16 V.

of this current increases from 0.911 at $V_3 = 0$ V to 1.138 at

$V_3 = 4$ V and this corresponds to a relative increase of 26 percent

compared with the value of 35.7 percent for the pin diode at 28 V.

This implies that the third-harmonic voltage may not enhance the

third-harmonic current in a short-length pin diode as greatly as

it does in a long-length pin diode.

The fundamental efficiency remains negative for most operating

conditions shown in Fig. 2.62. This property guarantees that the

passive mode operation can be achieved easily in pin diode 2. It is

noted that the fundamental efficiency becomes positive only at high

V_3 for θ_{3V} varying from -240 to 30 degrees, but the third-harmonic

efficiency at these conditions may be negative. There is no possibil-

ity to operate diode 2 at these conditions. Since the fundamental

current has a smaller phase delay than that in pin diode 1, the

fundamental efficiency can achieve a higher negative value. The

third-harmonic efficiency is also higher than that in diode 1. For

instance, the maximum third-harmonic efficiency found in Fig. 2.62

is 8.63 percent, compared with 5.67 percent achieved in diode 1 for

the case shown in Fig. 2.57. This is attributed to the larger

normalized third-harmonic current available in pin diode 2.

The third-harmonic power density and conversion efficiency,

shown in Figs. 2.63 and 2.64, respectively, are chosen according to

the same principle mentioned in the last section. The third-harmonic

power shows a similar dependence on the dc current density and

third-harmonic voltage as in diode 1. If compared at the same third-

harmonic voltage and V_1(diode 2) $= V_2$(diode 1)$/2$, the third-harmonic

power is not double that achieved in diode 1, despite the fact that the
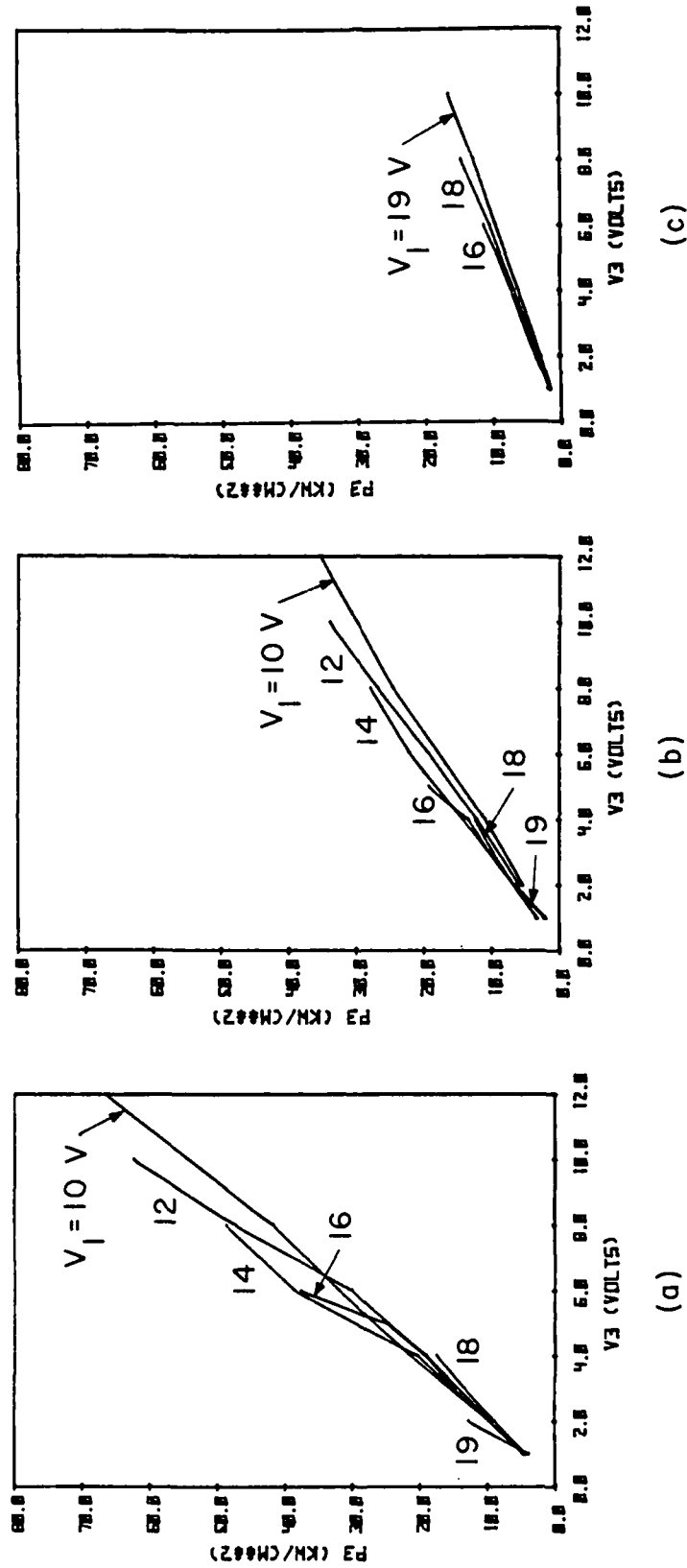
FIG. 2.63 THIRD-HARMONIC POWER DENSITY ACHIEVED IN pin DIODE 2 AT VARIOUS CONDITIONS.

(a) J_{dc} = 15 kA/cm^2, (b) J_{dc} = 7.5 kA/cm^2 AND (c) J_{dc} = 3.6 kA/cm^2.
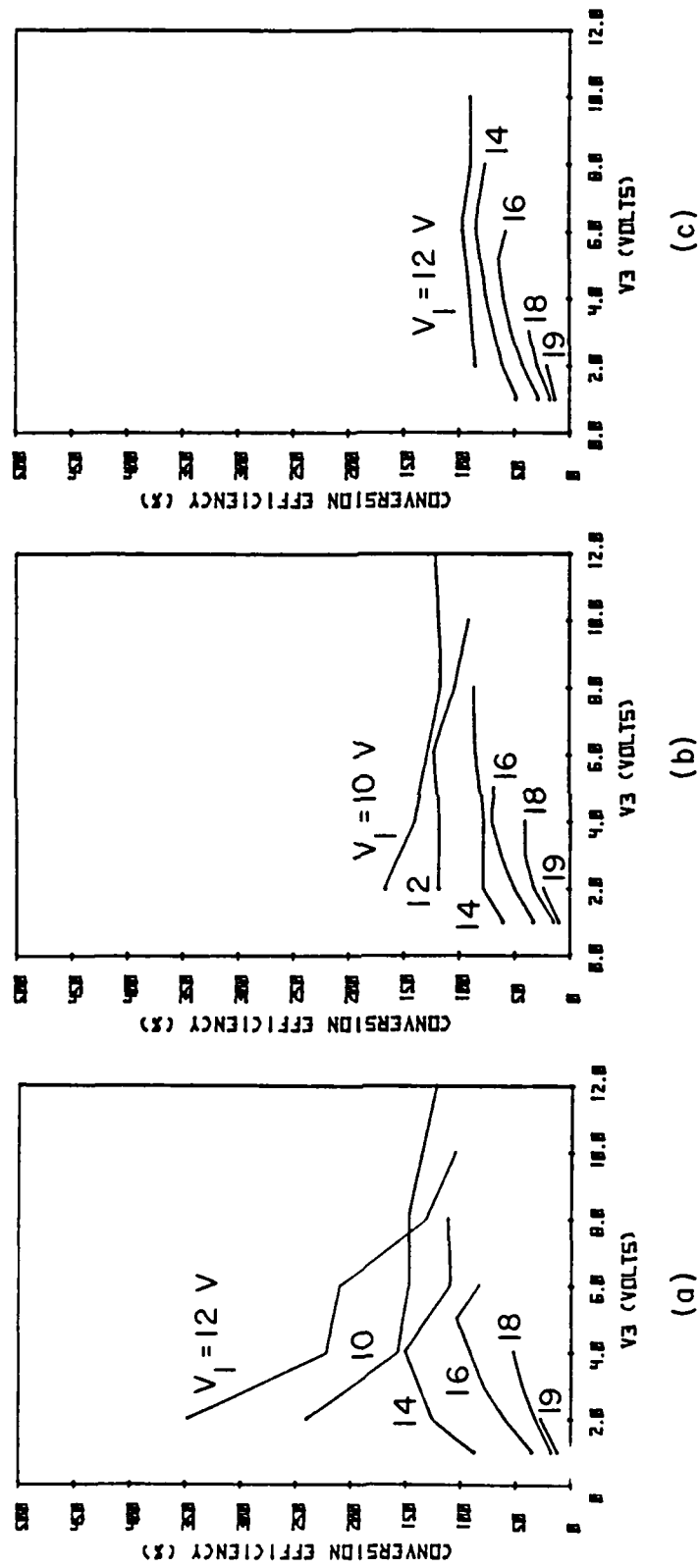
FIG. 2.64 CONVERSION EFFICIENCY ACHIEVED IN pin DIODE 2 AT VARIOUS CONDITIONS.

(a) J_{dc} = 15 kA/cm^2, (b) J_{dc} = 7.5 kA/cm^2 AND (c) J_{dc} = 3.6 kA/cm^2.

third-harmonic current is two times higher than that in diode 1.

The reasons for this are that, for diode 2, the fundamental efficiency

is always negative with a large magnitude for most operating condi-

tions; hence, for given V_1 and V_3, the data points chosen for

comparison are close to the maximum third-harmonic resistance points

where the corresponding phase difference $\theta_{3V} - \theta_{3I}$ is often below

150 degrees. However, the data point chosen for pin diode 1 for

given V_1 and V_3 is close to the maximum third-harmonic power point

where $\theta_{3V} - \theta_{3I}$ is near 180 degrees. Therefore, the third-harmonic

power achieved in diode 2 is higher than that in diode 1, but is not

double that in diode 1, while comparing at the same harmonic voltage.

Pin diode 2 has a small back-bias effect due to its short length.

Comparing at V_1 (diode 2) = V_1 (diode 1)/2, diode 2 can have a higher

V_3/V_1 than diode 1. This means that diode 2 can reach a higher

harmonic power density at higher V_3.

The conversion efficiency is quite different between the two

diodes. For diode 2, the conversion efficiency shows increasing

behavior at small V_3 but decreasing behavior at high V_3, except for

V_1 less than 12 V. This property can be understood in terms of

device characteristics in single-frequency operation, which indicates

that the fundamental efficiency is below zero for V_1 greater than

14 V. Hence, for V_1 greater than 14 V, a third-harmonic voltage

may not bring down the fundamental efficiency as rapidly as it brings

up the third-harmonic efficiency until V_3 is high. As a result,

the conversion efficiency has an increasing behavior at a small V_3.

For a given V_1 and V_3, the conversion efficiency is high for high

dc current density. This is related to the characteristics in

single-frequency operation that show that the fundamental efficiency is higher for higher dc current density. As a result, for given V_1, V_3, the fundamental efficiency after becoming negative is always small in magnitude at high dc current densities and thus the conversion efficiency is high. The behavior of the fundamental and third-harmonic resistances at $J_{dc} = 7.5$ kA/cm^2 are those of pin diode 1 shown in Fig. 2.62. As explained before, the fundamental resistance increases in magnitude with increasing V_3, but the third-harmonic resistance decreases in magnitude. The magnitudes of both resistances depend on how they are chosen. For the data points chosen for comparsion, the phase difference $\theta_{3V} - \theta_{3I}$ is less than 150 degrees. This might lead to the significant reduction of the susceptance B_{d3} at small V_3, despite the fact that the device length is also short. Hence, the magnitude of third-harmonic resistance may become higher at small V_3 than for that of diode 1.

At first the third-harmonic power is calculated by considering the circuit-matching effect only. Table 2.23 presents the results of the calculated third-harmonic power. As before, the third-harmonic power exhibits almost the same behavior with J_{dc} as that of pin diode 1 and is only slightly higher for $J_{dc} = 7.5$ kA/cm^2. In other words, a further reduction in device length may not improve the third-harmonic power output significantly. Increasing dc current density may only increase the output. This reveals a saturation phenomenon for the pin diode that will be discussed later.

Table 2.24 presents the maximum achievable third-harmonic power taking the thermal effect into consideration. Due to its low thermal resistance per unit area, pin diode 2 is not thermally

Table 2.23

Power Output for pin Diode 2 Taking into Account the Circuit-Matching Effect

V_1 (V)	V_3 (V)	J_{dc} (kA/cm²)	R_{d1} (Ω)	R_{d3} (Ω)	A (10^{-4} cm²)	V_{dc} (V)	Eff_{13} (%)	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
19.0	2.0	15.2	2.2	-1.0	1.39	21.45	27.75	45.3	1.777	5.2	4.0
13.0	3.0	15.0	1.4	-1.0	2.01	22.25	44.98	67.3	2.703	6.3	2.9
16.0	3.0	15.3	2.4	-1.0	1.74	23.58	30.02	62.5	2.601	5.9	3.2
14.0	6.0	15.3	21.5	-1.0	0.67	24.05	109.33	24.8	2.593	3.6	8.2
12.0	10.0	15.1	32.6	-1.0	0.36	23.43	104.88	12.5	2.221	2.7	16.2
10.0	6.0	15.0	26.2	-1.0	0.56	25.27	146.20	21.3	1.798	3.3	9.8
19.0	2.0	7.6	1.0	-1.9	0.56	21.21	24.15	9.0	0.356	3.3	20.1
18.0	4.0	7.7	1.5	-1.0	0.49	21.29	41.85	8.1	0.618	3.1	22.6
16.0	5.0	7.6	2.8	-1.0	0.36	23.18	67.46	6.3	0.689	2.7	30.5
14.0	6.0	7.6	4.7	-1.0	0.29	24.07	85.79	5.3	0.638	2.4	37.5
12.0	6.0	7.7	5.5	-1.0	0.28	24.86	123.39	5.4	0.543	2.4	38.1
10.0	8.0	7.6	18.0	-1.0	0.19	24.88	115.58	3.5	0.460	1.9	58.5
19.0	2.0	3.6	1.0	-2.3	0.19	21.03	21.73	1.5	0.057	2.0	121.0
18.0	3.0	3.6	1.0	-1.2	0.24	21.85	37.57	1.9	0.135	2.2	95.2
16.0	6.0	3.7	3.1	-1.0	0.14	22.45	56.81	1.1	0.155	1.6	163.1
14.0	8.0	3.7	5.5	-1.0	0.10	23.32	75.68	0.9	0.147	1.4	223.3
12.0	10.0	3.6	9.9	-1.0	0.07	23.56	91.22	0.6	0.120	1.2	324.1

Table 2.24

CW Power Output Results for pin Diode 2 Taking into Account Thermal Effects

J_{dc} (kA/cm²)	V_1 (V)	V_3 (V)	θ_{3V} (Deg.)	I_{dc} (A)	P_{dc} (W)	V_{dc} (V)	Eff_{13} (%)	R_{d1} (Ω)	R_{d3} (Ω)	P_3 (W)	D (mils)	R_{th} (°C/W)
15 - CM	10.0	12.0	120.0	0.16	3.67	23.21	121.98	84.79	-2.60	0.686	1.4	57.0
7.5 - CM	16.0	5.0	120.0	0.27	6.30	23.18	67.46	2.78	-1.00	0.689	2.7	27.7
3.6 - CM	16.0	6.0	150.0	0.05	1.12	22.45	56.81	3.08	-1.00	0.155	1.6	43.3
15 - DM	14.0	6.0	90.0	1.03	24.76	24.05	109.33	21.46	-1.00	2.593	3.6	7.7
7.5 - DM	16.0	5.0	120.0	0.27	6.30	23.18	67.46	2.78	-1.00	0.689	2.7	11.5
3.6 - DM	16.0	6.0	150.0	0.05	1.12	22.45	56.81	3.08	-1.00	0.155	1.6	22.1
15 - CR	12.0	10.0	120.0	0.49	11.51	23.43	104.88	35.56	-1.09	2.037	2.5	17.7
7.5 - CR	16.0	5.0	120.0	0.27	6.30	23.18	67.46	2.78	-1.00	0.689	2.7	16.8
3.6 - CR	16.0	6.0	150.0	0.05	1.12	22.45	56.81	3.08	-1.00	0.155	1.6	30.6
15 - DR	18.0	3.0	60.0	3.02	67.28	22.25	44.98	1.37	-1.00	2.703	6.3	2.5
7.5 - DR	16.0	5.0	120.0	0.27	6.30	23.18	67.46	2.79	-1.00	0.689	2.7	7.9
3.6 - DR	16.0	6.0	150.0	0.05	1.12	22.45	56.81	3.08	-1.00	0.155	1.6	16.2

restrained for J_{dc} less than 7.5 kA/cm². The maximum achievable

third-harmonic power output is 0.689 W for J_{dc} = 7.5 kA/cm² and

0.155 W for J_{dc} = 3.6 kA/cm². At J_{dc} = 15 kA/cm², the maximum

achievable power output depending on the heat sink structure used,

is the lowest for a single mesa on a copper heat sink (0.686 W) and

the highest for a ring geometry on a diamond heat sink (2.703 W).

2.4.6c Third-Harmonic Power Generation in pin Diode 3.

Due to its long device length, pin diode 3 exhibits a superior funda-

mental performance over other diodes, but its nonlinearity is ser-

iously degraded. In addition, its thermal resistance is high enough

to impose a constraint in the third-harmonic power output at high dc

currents. A brief discussion about its performance in the presence

of a third-harmonic voltage is given next.

Figure 2.65 shows the properties of pin diode 3 at V_1 = 38 V

and J_{dc} = 7.5 kA/cm². The diode experiences a small variation in the

fundamental and third-harmonic currents for V_3 below 6 V. At these

conditions, the third-harmonic efficiency is positive but small for

θ_{3V} between zero and 180 degrees and the corresponding fundamental

efficiency is still positive. This restrains the diode from operating

at lower V_3 to convert the external fundamental power to the third-

harmonic power. In other words, a very high V_3 is needed to shift

the induced current to the left such that the fundamental current

can have a phase delay less than 90 degrees. At such a condition,

the electric field in the central portion of the depletion region

for a certain θ_{3V} may fall below zero when the instantaneous terminal

voltage becomes low enough and causes the carriers to flow inwards

instead of outwards. As a consequence, the induced current contains
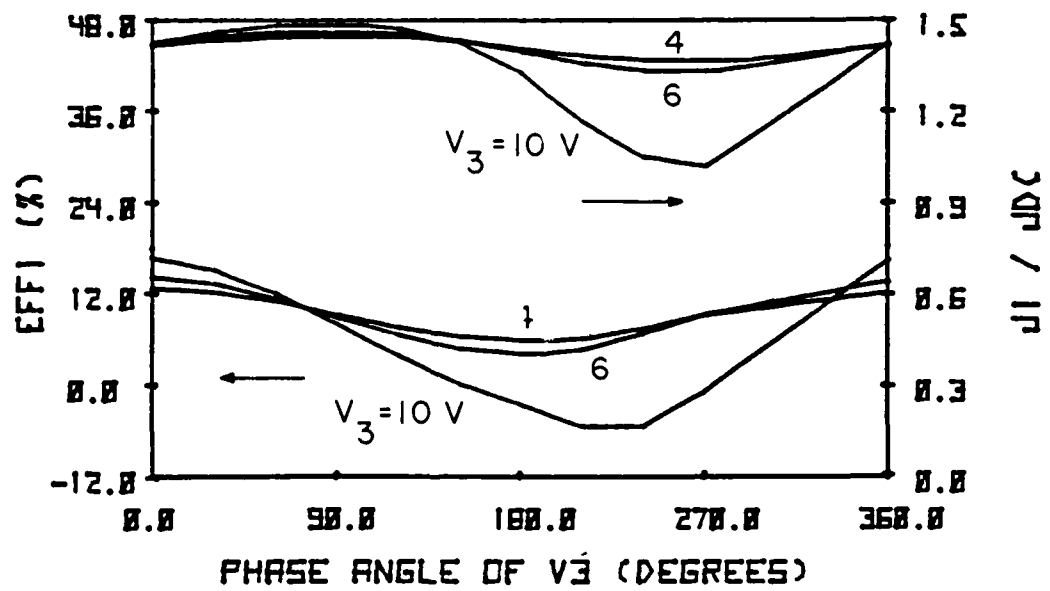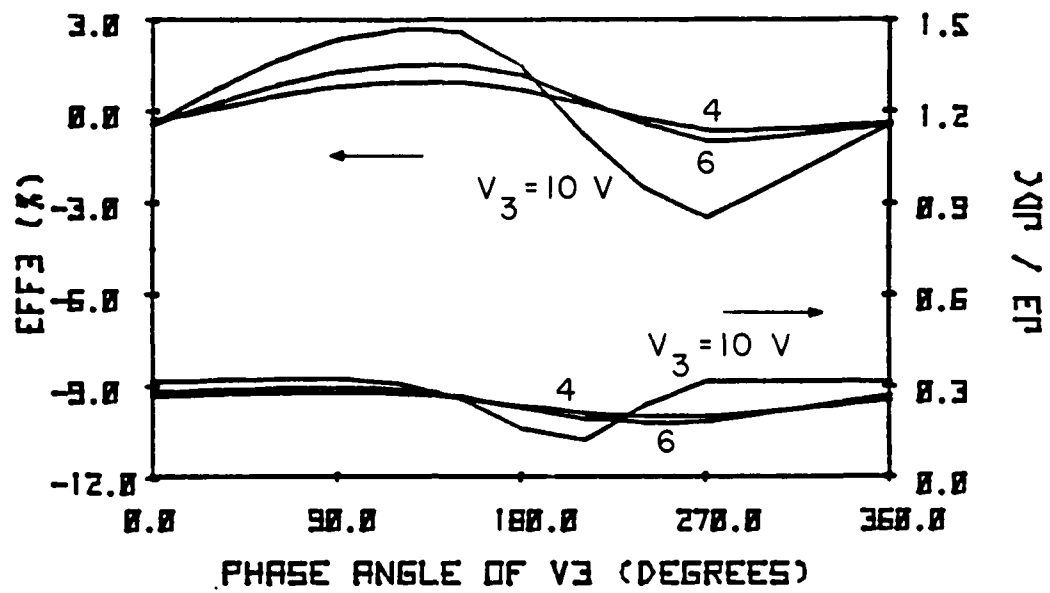
FIG. 2.65   FUNDAMENTAL AND THIRD-HARMONIC EFFICIENCIES AND

CURRENTS FOR pin DIODE 3 AT J_{dc} = 7.5 kA/cm^2 AND

V_1 = 38 V.

a dip that decreases the fundamental efficiency and enhances the third-harmonic current. From the results shown in Fig. 2.65, the above-mentioned phenomenon can occur at V_3 = 10 V for θ_{3V} between 210 and 270 degrees, for which the terminal voltage shows a significant negative peak between ωt = 180 and 270 degrees. In this interval the carrier concentration is still high and the corresponding third-harmonic efficiency is negative. Moreover, such a high V_3 causes a convergence problem in the simulation so it is impossible to utilize the phenomenon to enhance the third-harmonic power output.

Table 2.25 lists the calculated third-harmonic power output considering only the circuit-matching effect. The results also show the quadratic dependence of the third-harmonic power output on dc current density, but the required operating V_3 is high. The average power output level is much less than that in the other two diodes.

Table 2.26 presents the results including the thermal effect. For J_{dc} = 15 kA/cm^2, the thermal effect plays an essential role in restraining the third-harmonic power output. Instead, the maximum power output is achieved at J_{dc} = 7.5 kA/cm^2 and its value is only 0.23 W. It may be concluded that a long pin diode is not suitable for frequency multiplication.

2.4.7 Limitations on Third-Harmonic Power Generation from pin Diodes. From the results discussed previously, except for the thermal constraint, the maximum available third-harmonic power output from pin diodes for a given current density seems to saturate as the device length decreases. This saturation is the consequence of the behavior of the maximum available third-harmonic current from a pin diode. Due to its positive induced current, the normalized

Table 2.25

Power Output for pin Diode 3 Taking into Account the Circuit-Matching Effect

V_1 (V)	V_3 (V)	J_{dc} (kA/cm²)	R_{d1} (Ω)	R_{d3} (Ω)	A (10⁻⁴ cm²)	V_{dc} (V)	Eff_{13} (%)	P_{dc} (W)	P_3 (W)	D (mils)	R_{th} (°C/W)
40.0	5.0	15.3	1.6	-1.0	1.07	46.31	44.16	75.3	0.698	4.6	2.7
33.0	8.0	15.2	4.3	-1.0	0.63	48.22	68.30	46.3	0.731	3.5	4.3
36.0	10.0	15.2	8.9	-1.0	0.37	49.73	64.51	28.3	0.431	2.7	7.1
30.0	16.0	14.5	27.8	-1.0	0.23	51.16	89.59	17.2	0.385	2.1	11.7
24.0	20.0	14.6	100.1	-1.0	0.18	51.48	190.54	13.5	0.333	1.9	15.1
42.0	3.0	7.5	2.9	-1.0	0.27	44.83	4.06	9.2	0.026	2.3	20.7
40.0	8.0	7.5	1.0	-1.0	0.33	48.31	81.37	11.3	0.214	2.5	17.0
38.0	10.0	7.5	2.7	-1.0	0.17	49.16	51.96	6.2	0.088	1.8	32.3
35.0	12.0	7.6	1.9	-1.0	0.17	50.81	125.74	6.6	0.128	1.8	30.9
30.0	18.0	7.5	5.7	-1.0	0.16	51.67	153.36	6.1	0.230	1.3	33.6
24.0	22.0	7.6	15.7	-1.0	0.09	51.62	155.31	3.6	0.117	1.4	56.2
33.0	12.0	3.5	1.0	-2.0	0.06	50.36	250.34	1.1	0.033	1.1	184.0
35.0	14.0	3.7	1.0	-1.2	0.09	51.21	249.50	1.8	0.061	1.3	117.9
30.0	20.0	3.5	5.0	-1.0	0.06	50.93	120.03	1.1	0.045	1.1	184.5
24.0	24.0	3.5	10.7	-1.0	0.04	50.93	133.51	0.7	0.024	0.9	298.6

-210-

Table 2.26

Power Output for pin Diode 3 Taking into Account Thermal Effects

J_{dc} (mA/cm²)		V_1 (V)	V_3 (V)	θ_{3V} (Deg.)	I_{dc} (A)	P_{dc} (W)	V_{dc} (V)	Eff_{13} (%)	R_{d1} (Ω)	R_{d3} (Ω)	P_3 (W)	D (mils)	R_{th} (°C/W)
15	– CM	24.0	20.0	150.0	0.00	0.24	51.48	190.54	5597.05	-55.94	0.006	0.3	844.6
7.5	– CM	30.0	18.0	150.0	0.04	2.15	51.67	153.36	16.13	-2.84	0.081	1.0	95.3
3.6	– CM	36.0	14.0	150.0	0.03	1.75	51.21	249.50	1.00	-1.24	0.061	1.3	68.3
15	– DM	24.0	20.0	150.0	0.04	2.18	51.48	190.54	621.70	-6.21	0.054	0.8	93.8
7.5	– DM	30.0	18.0	150.0	0.12	6.09	51.67	153.36	5.69	-1.00	0.230	1.8	24.1
3.6	– DM	36.0	14.0	150.0	0.03	1.75	51.21	249.50	1.00	-1.24	0.061	1.3	36.5
15	– CR	24.0	20.0	150.0	0.02	0.80	51.48	190.54	1693.25	-16.92	0.020	0.5	255.5
7.5	– CR	30.0	18.0	150.0	0.12	6.09	51.67	153.36	5.69	-1.00	0.230	1.8	32.0
3.6	– CR	36.0	14.0	150.0	0.03	1.75	51.21	249.50	1.00	-1.24	0.061	1.3	46.9
15	– DR	24.0	20.0	150.0	0.14	7.20	51.48	190.54	188.03	-1.88	0.180	1.4	28.4
7.5	– DR	30.0	18.0	150.0	0.12	6.09	51.67	153.36	5.69	-1.00	0.230	1.8	18.7
3.6	– DR	36.0	14.0	150.0	0.03	1.75	51.21	249.50	1.00	-1.24	0.061	1.3	29.4

third-harmonic current, according to Eq. 2.23, never exceeds two and this means that the third-harmonic current will not increase significantly as the device length decreases greatly. Therefore, at a small device length, reduction in the required area for matching $1-\Omega$ resistance will decrease the third-harmonic power output. However, at large device length, the third-harmonic current usually increases at a rapid rate as the length decreases. The power output increases when the device length decreases since the third-harmonic current can increase at a faster rate. As a result, the maximum available third-harmonic power output at a given dc current density saturates for a certain device length. The condition for the saturation in the power output can be derived for an ideal situation. If the effect of the third-harmonic voltage is neglected and the phase difference $\theta_{3V} - \theta_{3I}$ is kept at 180 degrees, then Eq. 2.68 becomes

$$P_{3out} = \frac{1}{2} J_{dc}^2 \frac{J_{3N}^2}{G_{d3}^2 + B_{d3}^2} \quad , \qquad (2.69)$$

where $B_{d3} = (3\omega\varepsilon/w)$. Since the term $3\omega\varepsilon/w$ is always dominant in the denominator, provided that V_3 is not too small, the above equation can be approximated as

$$P_{3out} = \frac{1}{2} J_{dc}^2 \frac{J_{3N}^2 w^2}{9\omega^2\varepsilon^2} \quad . \qquad (2.70)$$

From the assumption that J_{3N} is only a function of device length, the saturation condition for P_{3out} is

$$\frac{dP_{3out}}{dw} = \frac{J_{dc}^2}{9\omega^2\varepsilon^2} \left(J_{3N} w^2 \frac{dJ_{3N}}{dw} + J_{3N}^2 w \right) = 0 \quad , \qquad (2.71)$$

i.e.,

$$\frac{1}{J_{3N}} \frac{dJ_{3N}}{dw} + \frac{1}{w} = 0 . \qquad (2.72)$$

This equation indicates that at the saturation condition the relative changing rate $(dJ_{3N}/dw)/J_{3N}$ should be equal to $-1/w$ and the slope dJ_{3N}/dw should be negative. The optimum device length W_{opt} corresponding to saturation in output power can be derived provided that the relation between J_{3N} and w is known. The case of $J_{dc} = 7.5$ kA/cm^2 is considered. Curve fitting J_{3N} corresponding to the maximum third-harmonic power output for three different pin diodes shown in Tables 2.21, 2.23 and 2.25, respectively yields

$$J_{3N}(w) = 2 \exp - (Aw^2 + Bw) , \qquad (2.73)$$

where $A = 0.1937 \times 10^{-8}$ cm^{-2} and $B = 0.8869 \times 10^{-4}$ cm^{-1}. Substituting $J_{3N}(w)$ into Eq. 2.72 yields $w_{opt} = 0.828$ μm. At this optimum length, J_{3N} is equal to 0.84 and the expected third-harmonic power outout according to Eq. 2.70 is 0.663 W, which is slightly less than the maximum value achieved in pin diode 2 at the same J_{dc}. This is because of the assumption of $\theta_{3V} - \theta_{3I} = 180$ degrees. Figure 2.66 shows the expected performance of a pin diode, based on Eqs. 2.70 and 2.73 along with the results achieved in pin diodes for comparison.

2.4.8 Summary and Conclusions. In addition to the ionization rates, space-charge and transit-time effects are important in the performance of pin diodes under breakdown conditions. They determine how fast the induced current builds up and falls off. For a long-length diode in single-frequency operation, both effects are significant in slowing down the build up and fall off of the
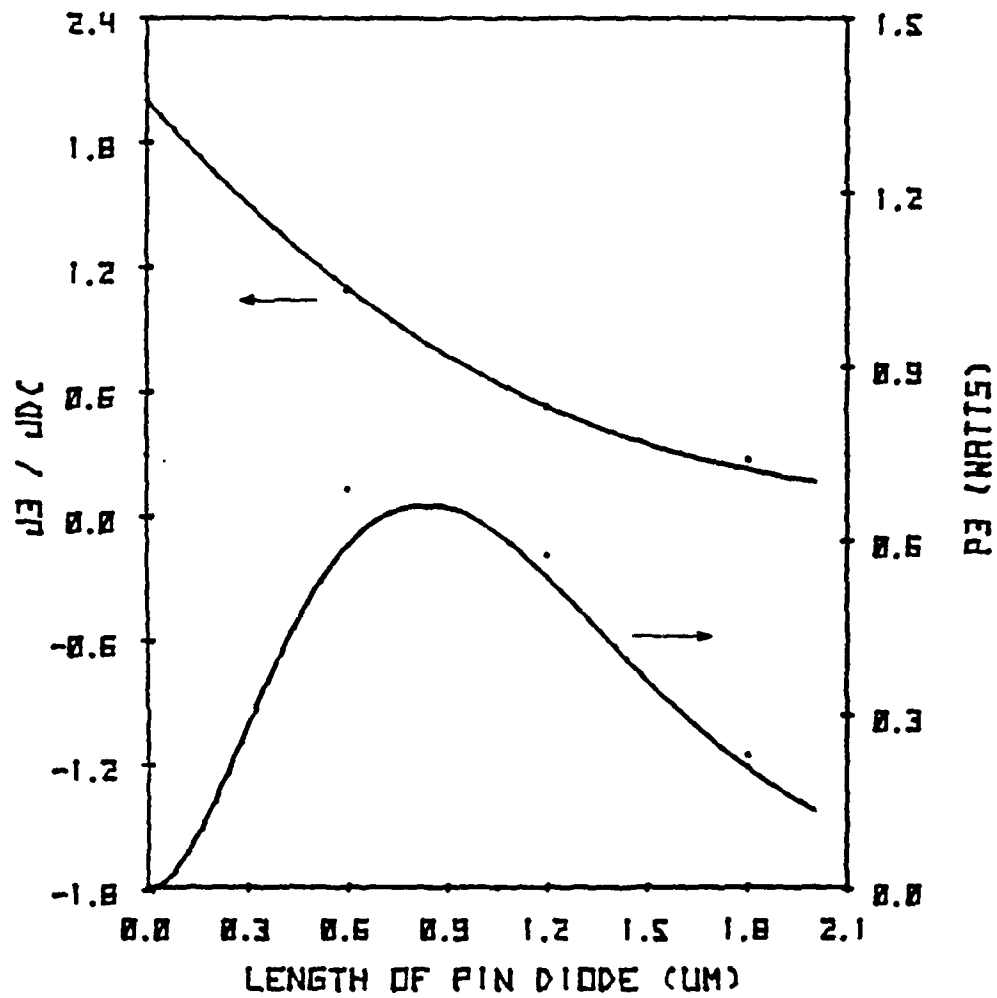
FIG. 2.66 CURVE FIT FOR OPTIMUM OUTPUT POWER CONDITIONS OF

pin DIODES AT J_{dc} = 7.5 kA/cm^2.

induced current. The result is that the fundamental efficiency is positive and high, but the harmonic current generation is degraded. For a short-length diode, the space-charge effect is not significant so the induced current is mainly determined by the ionization rates and the transit-time effect. The result is that the fundamental efficiency is reduced and may become negative for certain conditions, but the harmonic current generation is improved. However, significant improvement in the third-harmonic generation by further reducing the device length is impossible to achieve because the maximum third-harmonic current amplitude cannot exceed two times the dc current.

In multifrequency operation, a proper terminal voltage can further improve the shape of the induced current and shift it to the left to make the fundamental efficiency negative. Passive mode operation can be achieved easily for a short-length diode, but cannot be achieved for a long-length diode except with a large third-harmonic voltage. For interesting operating conditions, the third-harmonic current, which is not strongly dependent on the terminal voltage, can only be enhanced slightly by increasing the third-harmonic voltage. This property results in a maximum achievable third-harmonic power output, which is almost independent of the operating fundamental voltage, but is quadratically dependent on dc current density. Hence, it is better to operate pin diodes with a current density as high as possible until the thermal effect is not negligible.

The maximum achievable third-harmonic power output is limited due to the saturation behavior of the normalized third-harmonic current with device length. The optimum device length for which

the pin diodes can achieve the best third-harmonic power output in
passive mode operation is dependent upon the operating frequency
but seems independent of the dc current density if it is not too
high. For this particular frequency, 23 GHz, the optimum device
length is 0.828 μm and the corresponding transit time is approxi-
mately 0.38π. At high frequencies, the optimum device length
decreases proportionately and the maximum achievable third-
harmonic power decreases at a rate inversely proportional to the square
of frequency.

CHAPTER III

MODEL FOR SELF-OSCILLATING OPERATION OF THE THREE-FREQUENCY

IMPATT DIODE OSCILLATOR

3.1 Introduction

This section is concerned with an investigation of the third-harmonic performance of an IMPATT diode using an analytical approach. It was shown in the previous chapter that the harmonic current components exist in an IMPATT diode being driven with an arbitrary shape of RF voltage. Hence, in a practical IMPATT diode oscillator, owing to interaction between the fundamental and harmonic components through the device nonlinearity, there will be an observable effect on third-harmonic generation. Computer simulations presented in the previous chapter for two-frequency operation were not sufficiently detailed to provide the insight necessary to understand the diode performance in multifrequency operation. With operation involving more than two frequencies, computer simulation becomes very complicated since more variables are needed in order to determine an optimum performance at the third harmonic. Therefore, an alternative method for investigating multifrequency operation has been adopted, namely, an analytic approach has been developed with the equivalent circuit model for an IMPATT diode. Most of the analytic analyses[3,23,91] rely on using the exponential nonlinearity inherent in the avalanche breakdown, but they neglect depletion-layer modulation effects as they are difficult to incorporate in these models. In the following study, Mouthaan's work has been adapted in developing the

-216-

three-frequency equivalent circuit model for a GaAs double-Read IMPATT diode. The circuit assumed also enables investigation of the conditions required for starting oscillation, stability criteria, and the effect of a loading resistance on the level of power generation at the third harmonic. Although this model is simplified and therefore less accurate than a computer simulation, it requires a shorter computation time and provides sufficiently good information about device-circuit interaction.

3.2 Equivalent Circuit Model for Three-Frequency Operation of an IMPATT Diode

The GaAs double-Read IMPATT diode having the same length for the p and n regions is used for an oscillator model. Similar to Read's original analysis,[3] the first step is to divide the entire space region of the device into an avalanche region of width x_a and two equal-length drift regions for electrons and holes, respectively. The following assumptions have also been made:

1. The space-charge effect and depletion-layer modulation are totally neglected. Electrons and holes travel at the saturated velocity v_s.

2. The ionization rates for both carriers are the same and the ambient temperature of the device is $500°K$.

3. The conduction current in the avalanche region is constant (independent of position). According to Read's analysis,[3] the injected current density J_{inj} can be expressed as

$$J_{inj} = J_{co} \exp\left(\frac{2\alpha'}{\tau_a}\int_0^t V_a \, dt\right) \quad , \qquad (3.1)$$

where $\tau_a = x_a/v_s$ and V_a is the RF voltage across the avalanche region. The total current density J_t, which is the sum of the injected current and displacement current densities, is

$$J_t = J_{inj} + C_a \frac{dV_a}{dt} \quad . \qquad (3.2)$$

4. The spatial distribution of carriers injected into the drift regions remains unchanged over the drift time in both regions. Assuming that the metallurgical junction is located at $x = 0$, the spatial distribution of electron and hole currents, J_{nd} and J_{pd}, respectively, are

$$J_{nd}(x,t) = J_{inj}(t - x/v_s) \quad x_a/2 < x < w/2 \qquad (3.3)$$

and

$$J_{pd}(x,t) = J_{inj}(t + x/v_s) \quad -w/2 < x < -x_a/2 \quad , \qquad (3.4)$$

where w is the total width of the device. Furthermore, the carriers in the avalanche region are assumed to have no contribution to the induced current, so the total current density can also be expressed as

$$J_t = \frac{1}{2\ell_d}\int_{x_a/2}^{w/2} J_{nd} \, dx + \frac{1}{2\ell_d}\int_{-w/2}^{-x_a/2} J_{pd} \, dx + C_d \frac{dV_d}{dt}$$

$$= \frac{1}{\ell_d}\int_{x_a/2}^{w/2} J_{inj}\left(t - \frac{x}{v_s}\right) dx + C_d \frac{dV_d}{dt} \quad , \qquad (3.5)$$

where ℓ_d is the drift region length, $C_d = \epsilon/2\ell_d$ and V_d is the total RF voltage across both drift regions. In operation at an angular frequency ω, the current density J_{inj} can be expressed in terms of a Fourier series as follows:

$$J_{inj} = J_{dc}\left[1 + \frac{1}{2}\sum_{m=1}^{\infty}[\beta_m \exp(jm\omega t) + \beta_m^* \exp(-jm\omega t)]\right] \quad .$$

(3.6)

The normalized mth component of the current phasor b_m can be expressed in the following form:

$$\beta_m = \frac{\frac{1}{\pi}\int_0^{2\pi} J_{inj}\exp(-jm\omega t)\,d\omega t}{J_{dc}} = \frac{2\int_0^{2\pi} J_{inj}\exp(-jm\omega t)\,d\omega t}{\int_0^{2\pi} J_{inj}\,d\omega t} \quad .$$

(3.7)

Since J_{inj} is always positively defined, Eq. 3.7 implies that

$$|\beta_m| \leqq 2 \quad .$$

(3.8)

Since the total current must be the same at either the avalanche region or the drift region, Eqs. 3.2 and 3.5 imply that the mth harmonic phasor component J_{tm} of the total current can be expressed as follows:

$$J_{tm} = J_{dc}\beta_m + jm\omega C_a V_{am} = \frac{1 - \exp(-jm\theta_d)}{jm\theta_d}J_{dc}\beta_m + jm\omega C_d V_{dm} \quad ,$$

(3.9)

where V_{am} and V_{dm} are the mth harmonic phasor of V_a and V_d, respectively, and $\theta_d = \omega\ell_d/v_s$. The assumed electric field profile of the diode is shown in Fig. 3.1a and the equivalent circuit for the
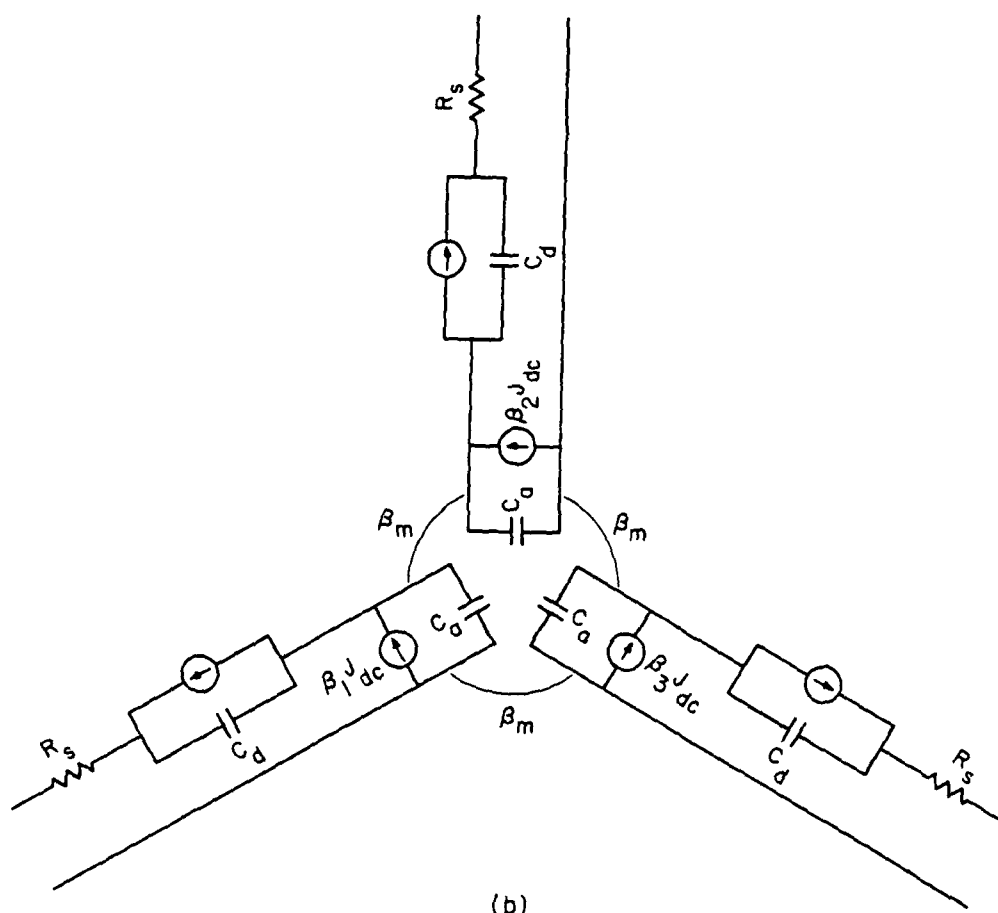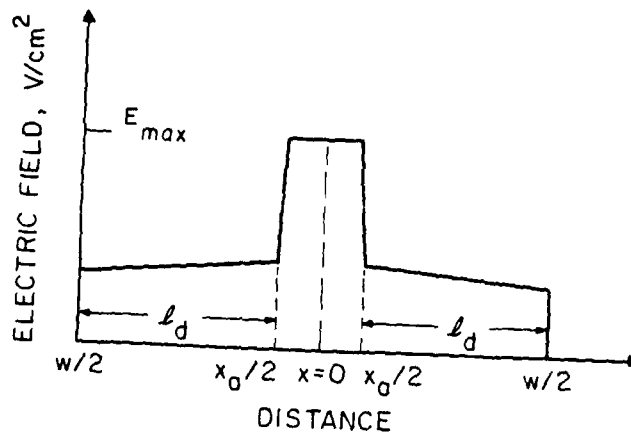
FIG. 3.1 (a) ELECTRIC FIELD PROFILE FOR THE DIODE AND (b)

EQUIVALENT CIRCUIT FOR THREE-FREQUENCY OPERATION.

[$f \approx 23$ GHz, $x_a = 0.2$ μm, $\theta_d = \omega(\ell/v_s) = 0.74\pi$, $v_s =$

5.2×10^6 cm/s, $\alpha' = 0.22$ V^{-1}cm^{-1}, $E_{max} = 5 \times 10^5$ V/cm

AND $A = 1.55 \times 10^{-4}$ cm^2]

fundamental second- and third-harmonic signal components is shown
in Fig. 3.1b. In the equivalent circuit assumed in this analysis,
the avalanche region at each frequency is modeled by a current gen-
erator in parallel with an avalanche region actual capacitance. The
drift region is modeled by a dependent current source in parallel
with a drift region actual capacitance. The coupling between each
harmonically related signal is assumed to be through the term being
a nonlinear function of V_{am}.

With the aid of the equivalent circuit, the device impedance
Z_{dm} at the mth harmonic frequency, defined by the ratio of the mth
harmonic phasor of the terminal voltage to the mth harmonic phasor of
the total current, can be written as follows:

$$Z_{dm} = \frac{V_{am} + V_{dm}}{A(J_{dc}\beta_m + jm\omega C_a V_{am})} . \tag{3.10}$$

When V_d is expressed in terms of V_a and Eq. 3.9 is used, the impedance
Z_{dm} can be expressed as follows:

$$Z_{dm} = \frac{1}{jmCA} \frac{1}{1 + J_{dc}\beta_m/jm\omega C_a V_{am}} + \frac{1 - [1 - \exp(-jm\theta_d)]/jm\theta_d}{jm\omega C_a A(1 + jm\omega C_a V_{am}/J_{dc}\beta_m)} , \tag{3.11}$$

where $C = C_a C_d/(C_a + C_d)$ is the total capacitance of the device.

In an actual oscillator circuit, the diode is connected to its
external linear circuit with the impedance $Z_{cm} = R_{cm} + jX_{cm}$ deter-
mined at frequency $m\omega$. The condition for a stable oscillation
requires that the total impedance Z_{tm} vanish at frequency ω, i.e.,

$$Z_{tm} = Z_{dm} + Z_{cm} = 0 . \tag{3.12}$$

The diode impedance Z'_{dm} is defined as

$$Z'_{dm} = \frac{1}{jm\omega C_d A}\left[1 - \frac{1 - \exp\left(-jm\theta_d\right)}{jm\theta_d}\right] \tag{3.13}$$

and the diode-circuit coefficient ρ_m is defined as

$$\rho_m = \frac{Z'_{dm} + Z_{cm}}{Z_{cm} + \frac{1}{jmCA}} \quad . \tag{3.14}$$

Equation 3.12, rewritten in terms of the ratio $J_{dc}\beta_m/jmC_a V_{am}$, yields the following equation for an oscillation condition:

$$\frac{jm\omega C_a V_{am}}{J_{dc}\beta_m} = -\rho_m. \tag{3.15}$$

The preceding equation states that the ratio of the displacement current to the injected current in the avalanche region is restricted by the value of the parameter ρ_m. The parameter ρ_m, defined by Eq. 3.14, describes the combined impedance characteristics of the external circuit, the drift region, and the total capacitance of the diode. Solutions to the oscillation equation (Eq. 3.15) can exist only for a particular value of ρ_m. One fundamental limitation of the possible solutions of Eq. 3.15 results from the fact that the magnitude of β_m is less than two, which means that the magnitude of the required ρ_m value should be greater than a certain value. The other limitation is due to the permissible RF voltage swing which cannot exceed the dc bias voltage, otherwise depletion-layer modulation will take place. These limitations of the solutions restrict the available output power from the device. The useful output power P_m is, therefore, given by

$$P_m = 0.5 \, |J_{tm}^2| R_{cm} \qquad (3.16)$$

or

$$P_m = 0.5 \, |\rho_m - 1|^2 \, |\beta_m|^2 J_{dc}^2 R_{cm} \qquad (3.17)$$

if J_{tm} is replaced by ρ_m and β_m.

The coefficient β_m can be calculated from Eq. 3.7 if the value of V_{am} is known. It is of particular interest to consider the inductive type of injection, which makes the coefficient β_m purely imaginary and the coefficient ρ_m real if V_{am} is real. This also makes it possible to discuss the small-signal oscillation approximation.

3.3 Small-Signal Oscillation Conditions

In order to solve the oscillation equation (Eq. 3.15) for small-signal conditions, the Fourier series representation must be obtained for the injected current density J_{inj} involving the Fourier coefficients being related to the voltage V_a across the avalanche region. If $V_a(t)$ (the instantaneous voltage across the avalanche region) is assumed to be

$$V_a(t) = \sum_{m=1}^{\infty} V_a \sin(m\omega t + \phi_m) \quad , \qquad (3.18)$$

the complex form of V_a is therefore

$$V_a(t) = \sum_{m=1}^{\infty} \left[\frac{V_a}{2j} e^{j\phi_m} e^{jm\omega t} - \frac{V_a}{2j} e^{-j\phi_m} e^{-jm\omega t} \right] \quad . \qquad (3.19)$$

Defining the normalized mth harmonic voltage yields

$$v_{am} = \frac{2\alpha' V_{am}}{m\omega \tau_a} e^{j\phi_m} \qquad (3.20)$$

and carrying out the integration of Eq. 3.1 yields

$$J_{inj} = J_{co} \exp \left(\sum_{m=1}^{\infty} |v_{am}| [\cos \phi_m - \cos (m\omega t + \phi_m)] \right)$$

$$= J_{co} \exp \left(\sum_{m=1}^{\infty} |v_{am}| \cos \phi_m \right) \exp \left(- \sum_{m=1}^{\infty} |v_{am}| (\cos m\omega t + \phi_m) \right) .$$

(3.21)

This series expansion fully describes the dc current as well as harmonic current components. It can be seen that the dc current density can be made independent of v_{am}, if the diode is biased using a constant current source. Based on the preceding, the oscillation equation (Eq. 3.15) can be rewritten as follows:

$$- \frac{\beta_m}{v_{am}} = \frac{m^2 X}{\rho_m} ,$$

(3.22)

where $X = (\omega^2 / \omega_a^2)$ is the square of the ratio of the fundamental frequency to the avalanche resonant frequency $\omega_a = \sqrt{2\alpha' J_{dc} \epsilon / v_s}$. It is assumed that the diode is terminated by an external circuit with the impedance Z_{cm} and is required to operate at the frequency ω. For a small dc current density, the total resistance of the oscillator circuit is positive, so no oscillation will occur. If the dc current density is increased to a certain value J_{dcs}, the device negative resistance becomes equal to the load resistance and the oscillation process will be initiated. This is a start-oscillation condition and, correspondingly, the oscillation signals are small in magnitude. For the case $m = 1$, $b_1 = - v_{a1}$, which implies that ρ_1 is real. The definition of ρ_1 leads to the following equations:

$$X_{c1} = \frac{1}{\omega CA} + (R_s + R_{c1})\left[\cot\frac{\theta_d}{2} + \frac{C_d}{C_a}\frac{\theta_d/2}{\sin^2\left(\frac{\theta_d}{2}\right)}\right] \qquad (3.23)$$

and

$$\rho_1 = X_s = \frac{\omega^2}{\omega_a^2} = 1 + \frac{1}{\omega C_d A(R_s + R_{c1})}\frac{\sin\left(\frac{\theta_d}{2}\right)}{\theta_d/2} \quad . \qquad (3.24)$$

Since ρ_1 is related to the dc current density, the required dc current density for achieving the preceding condition is

$$J_{dcs} = \frac{\epsilon\omega^2}{2\alpha' v_s \rho_1} = \frac{\epsilon}{2\alpha' v_s}\frac{\omega^2}{1 + \frac{1}{m\omega C_d A(R_s + R_{c1})}\frac{\sin^2\left(\frac{\theta_d}{2}\right)}{\theta_d/2}} \quad .$$

$$(3.25)$$

To start oscillation at the fundamental, second- and third-harmonics simultaneously, the following condition can be derived assuming that ρ_m is real and positive ($\phi_m = 0$ or 180 degrees) and also that there is no interaction among these signals. At $J_{dc} = J_{dcs}$ and $\rho_1 = X_s$ at the fundamental frequency, the circuit impedance at the harmonics should be chosen in such a way that the corresponding ρ_m is greater than $m^2\rho_1$. In other words, this requires that

$$X_{cm} = \frac{1}{m\omega CA} + (R_s + R_{cm})\left[\cot\left(\frac{m\theta_d}{2}\right) + \frac{C_d}{C_a}\frac{m\theta_d/2}{\sin^2\left(\frac{m\theta_d}{2}\right)}\right] \qquad (3.26)$$

and

$$1 + \frac{1}{m\omega C_d A(R_s + R_{c1})}\frac{\sin^2\frac{m\theta_d}{2}}{m\theta_d/2} \geqq m^2 X_s \quad . \qquad (3.27)$$

Substituting Eq. 3.24 into Eq. 3.27 and assuming that $m\omega A C_d (R_s + R_{cm})$ is much smaller than one yields

$$R_s \; \lesseqqgtr \; \frac{R_{c1} \cos^2 \left[(\theta_d/2)/4 \right] - R_{c2}}{1 - \cos^2 (\theta_d/2)/4} \qquad (3.28)$$

and

$$R_s \; \lesseqqgtr \; \frac{R_{c1} \left[1 - \frac{4}{3} \sin^2 (\theta_d/2) \right]^2 / 9 - R_{c3}}{1 - \left[1 - \frac{4}{3} \sin^2 (\theta_d/2) \right]^2 / 9} \quad . \qquad (3.29)$$

Since R_s is positive, the following must hold:

$$R_{c2} \; \lesseqqgtr \; R_{c1} \cos^2 (\theta_d/2)/4 \qquad (3.30)$$

and

$$R_{c3} \; \lesseqqgtr \; R_{c1} \left[1 - \frac{4}{3} \sin^2 (\theta_d/2) \right]^2 / 9 \quad . \qquad (3.31)$$

As a result, the loading condition for harmonics cannot be chosen arbitrarily. Considering that the diode has a transit angle θ_d of 0.74π at the fundamental frequency, the load resistance at the second and third harmonics must satisfy the following condition:

$$R_{c2} \; \lesseqqgtr \; 0.04 \, R_{c1} \qquad (3.32)$$

and

$$R_{c3} \; \lesseqqgtr \; 0.0017 \, R_{c1} \quad . \qquad (3.33)$$

The above lead to the following condition

$$R_s \; \lesseqqgtr \; 0.0017 \, R_{c1} \quad . \qquad (3.34)$$

The noninteraction between the fundamental and harmonic signals results in the requirement of a very small circuit resistance presented at harmonics for the start of oscillation. This is not,

however, easy to facilitate in practice. If the fundamental signal is increased, the interaction between the signals cannot be neglected and a significant improvement in the load resistance at the harmonics will be possible. Now, the relationship between v_{am} and the load resistance will be derived. It is assumed that ρ_m is real. The real ρ_m implies that v_{am} is also real. By proper design of the external circuit, v_{a1} can be made sufficiently large in magnitude, compared to the values of v_{a2} and v_{a3}. A Taylor series expansion for Eq. 3.21 results in the following set of equations:

$$\beta_1 = - v_{a1}\left[1 - \left(v_{a2} + \frac{v_{a3} v_{a2}}{v_{a1}} \right) + \frac{1}{2} v_{a1}^2 + ,\ldots, \right] \quad , \qquad (3.35)$$

$$\beta_2 = - v_{a2}\left(1 - \frac{v_{a1}^2}{v_{a2}} - \frac{v_{a1} v_{a3}}{v_{a2}} + ,\ldots, \right) \qquad (3.36)$$

and

$$\beta_3 = - v_{a3}\left(1 - \frac{v_{a2} v_{a3}}{v_{a3}} + ,\ldots, \right) \quad . \qquad (3.37)$$

Neglecting the higher-order terms in the preceding equations results in the following approximate equations:

$$1 - \left(v_{a2} + \frac{v_{a2} v_{a3}}{v_{a1}} \right) + \frac{1}{2} v_{a1}^2 = \frac{X_s}{\rho_1} \quad , \qquad (3.38)$$

$$1 - \left(\frac{1}{2} \frac{v_{a1}^2}{v_{a2}} - \frac{v_{a1} v_{a3}}{v_{a2}} \right) = \frac{4X_s}{\rho_1} \qquad (3.39)$$

and

$$1 - \frac{v_{a1} v_{a2}}{v_{a3}} = \frac{9X_s}{\rho_1} \quad . \qquad (3.40)$$

For a given frequency and load resistance, the preceding equations can be solved for v_{am}. For the diode shown in Fig. 3.1 with $J_{dc} = 1256$ A/cm^2, $f_1 = 23$ GHz and $R_s = 0\ \Omega$, the solution for v_{am} at a

certain load condition is presented in Fig. 3.2. It can be seen from that figure that as long as R_{c3} is not too small, v_{a3} (negative) is several orders of magnitude smaller than v_{a1} and v_{a2}. Therefore, the terms in Eqs. 3.38 and 3.39 associated with v_{a3} can be neglected which leads to an explicit expression for v_{am} in terms of ρ_m, namely,

$$v_{a2} = \frac{1 - X_s/\rho_1}{4X/\rho_2} \quad , \tag{3.41}$$

$$v_{a1}^2 = \frac{2(1 - 4X_s/\rho_2)[1 - (X_s/\rho_1)]}{4X_s/\rho_2} \tag{3.42}$$

and

$$v_{a3} = \frac{v_{a2}v_{a1}}{1 - 9X_s/\rho_3} \quad . \tag{3.43}$$

Since ρ_1 is assumed to be slightly greater than X_s, Eq. 3.41 implies that v_{a2} should be positive. From Eq. 3.42 the real value of v_{a1} can be obtained only if $\rho_2 - 4X_s \geqq 0$. According to Eqs. 3.24 and 3.27 this leads to the condition that $R_{c2} \leqq 0.04\ R_{c1}$, which explains the choice of $R_{c2} = 0.02\ \Omega$ value in this example presented for solving v_{am}. For positive values of v_{a1}, v_{a3} becomes negative if R_{c3} is large.

In conclusion, for a real and positive ρ_m, nonvanishing solutions of v_{am} at small-signal conditions can exist only for certain load conditions. For a complex ρ_m, it is not feasible to determine an analytic form of solution for v_{am}. By reducing R_{c1} or increasing J_{dc}, v_{a1} will increase rapidly and the range of large-signal operation is entered.
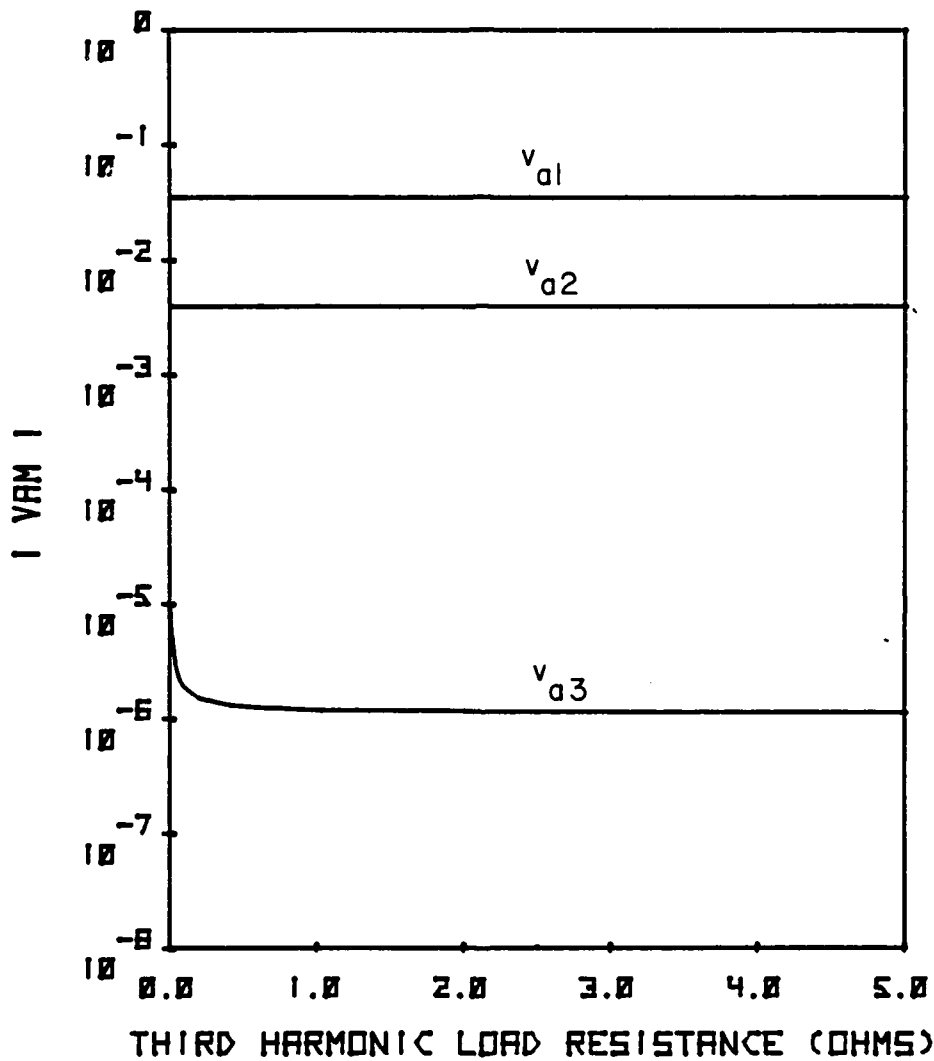
FIG. 3.2 SOLUTIONS FOR v_{am} AT SMALL-SIGNAL CONDITION WITH

$R_{c2} = 0.02 \ \Omega$, $R_{c1} = 0.64 \ \Omega$, $J_{dc} = 1256 \ A/cm^2$ AND

$f = 23$ GHz.

3.4 Stability Conditions for Three-Frequency Operation

The stability is essential in designing a negative-resistance oscillator. For a single-frequency oscillator, the stability criterion is formulated as $(\partial R_t/\partial V)(\partial X_t/\partial \omega) - (\partial X_t/\partial V)(\partial R_t/\partial \omega) > 0$. In the simplest case where the device has a frequency independent impedance, it is presented with a general external network being frequency dependent and the stability criterion becomes $\partial |R_t|/\partial V \lesseqgtr 0$ which means that the negative device resistance must decrease with increasing voltage amplitude. For a multifrequency oscillator, the mutual interaction between signals and the circuit coupling at the harmonic frequencies have certain effects on the stability of the oscillator. Based on the work of Kurokawa[92] and Bates and Khan,[93] the stability criterion required for multifrequency oscillators can be formulated. This section follows their work in the derivation of the stability criteria for a general three-frequency IMPATT oscillator.

In general, to derive the stability criteria, a small perturbation to the oscillation condition is applied. It is assumed that the time-varying voltage $V_a(t)$ across the avalanche region is given by

$$V_a(t) = \sum_{m=1}^{3} V_{am} \sin [\omega_m t + \phi_m(t)] , \qquad (3.44)$$

where $\omega_m = m\omega_1$ exists at the steady state. The fundamental voltage phase angle ϕ_1 is arbitrarily chosen and it has a nonzero value. Under the perturbation conditions the rate of change of the phase angle with respect to time is equal to the real part of the frequency

deviation. If $R_m = \text{Re } (\beta_m/v_{am}) + (m^2 X/\rho_m)$ and $K_m = \text{Im } (\beta_m/v_{am}) + (m^2 X/\rho_m)$, the oscillation condition can be written as

$$R_m + jK_m = 0 \ . \tag{3.45}$$

At a stable operation point, $R_m = R_{mo}$ and $K_m = K_{mo}$. When the steady-state oscillation condition is perturbed, i.e., R and K can be represented by

$$R_m = R_{mo} + dR_m \tag{3.46}$$

and

$$K_m = K_{mo} + dK_m \ , \tag{3.47}$$

then the corresponding perturbation of the voltage, frequency and phase angle are denoted by δV_{ak}, $\delta\omega_k$ and $\delta\phi_k$, respectively. For a small and time invariant perturbation, the Taylor series expansion can be applied to the oscillation equation (Eq. 3.45) and results in

$$d(R_m + jK_m) = \sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial V_{ak}} + j \frac{\partial K_m}{\partial V_{ak}} \right) \delta V_{ak} + \sum_{k=1}^{3} \left(\frac{\partial R_m}{\delta\phi_k} + j \frac{\partial K_m}{\delta\phi_k} \right) \delta\phi_k$$

$$+ \sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial\omega_k} + j \frac{\partial K_m}{\partial\omega_k} \right) \delta\omega_k \ . \tag{3.48}$$

This equation is not valid if the perturbation is time dependent since the signal components cannot be defined explicitly. If the oscillation is nearly at the steady-state condition, the Fourier analysis can be applied for expressing the oscillating signals. Under this nearly steady-state condition, δV_{ak}, $\delta\omega_k$ and $\delta\phi_k$ are small time-varying functions. To study the stability criterion,

Bates and Khan[92] extended Kurokawa's work to include the δV_{ak} and $\delta \phi_k$ to $\delta \omega_k$ perturbations in the following way:

$$\delta \omega_k = \frac{d(\delta \phi_k)}{dt} - j \frac{1}{V_{ak}} \frac{d(\delta V_{ak})}{dt} \qquad (3.49)$$

and assumed that $\omega_k = k \omega_1$ is still held under small time-varying perturbations. Using the preceding relationship yields

$$\frac{d(\delta \phi_k)}{dt} - j \frac{1}{V_{ak}} \frac{d(\delta V_{ak})}{dt} = k \left(\frac{d(\delta \phi_1)}{dt} - j \frac{1}{V_{a1}} \frac{d(\delta V_{a1})}{dt} \right) . \qquad (3.50)$$

Equating the real and imaginary parts of Eq. 3.50 and integrating them with respect to time yields

$$\delta \phi_k = k \delta \phi_1 + a_k \qquad (3.51)$$

and

$$\frac{\delta V_{ak}}{V_{ak}} = k \frac{\delta V_{a1}}{V_{a1}} + b_k , \qquad (3.52)$$

where a_k and b_k are integration constants and a_1, b_1 are both zero. Defining $\delta \overline{V}_{ak} = \left(\delta V_{ak} / V_{ak} \right)$ and substituting Eqs. 3.51 and 3.52 into Eq. 3.50 results in

$$\sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial \overline{V}_{ak}} + j \frac{\partial K_m}{\partial \overline{V}_{ak}} \right) (k \delta \overline{V}_{a1} + b_k) + \sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial \phi_k} + j \frac{\partial K_m}{\partial \phi_k} \right) (k \delta \phi_1 + a_k)$$

$$+ \sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial \omega_k} + j \frac{\partial K_m}{\partial \omega_k} \right) \left(\frac{d(\delta \phi_k)}{dt} - j \frac{d(\delta \overline{V}_{ak})}{dt} \right) = 0 . \qquad (3.53)$$

Since the operating point is independent of the choice of the reference fundamental voltage phase angle ϕ_1, it is required that

$$\frac{dR_m}{d\phi_1} = \sum_{k=1}^{3} k \frac{\partial R_m}{\partial \phi_k} = 0 \qquad (3.54)$$

and

$$\frac{dK_m}{d\phi_1} = \sum_{k=1}^{3} k \frac{\partial K_m}{\partial \phi_k} = 0 \quad . \qquad (3.55)$$

By using the preceding relations, Eq. 3.53 becomes

$$\sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial \overline{V}_{ak}} + j \frac{\partial K_m}{\partial \overline{V}_{ak}} \right) (k \delta \overline{V}_{a1} + b_k) + \sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial \phi_k} + j \frac{\partial K_m}{\partial \phi_k} \right) a_k$$

$$+ \sum_{k=1}^{3} \left(\frac{\partial R_m}{\partial \omega_k} + j \frac{\partial K_m}{\partial \omega_k} \right) k \left(\frac{d(\delta \phi_1)}{dt} - j \frac{d(\delta \overline{V}_{a1})}{dt} \right) = 0 \quad . \quad (3.56)$$

Equating the real and imaginary parts to zero results in

$$\sum_{k=1}^{3} k \frac{\partial R_m}{\partial \overline{V}_{ak}} \delta \overline{V}_{a1} + \sum_{k=1}^{3} \frac{\partial K_m}{\partial \omega_k} \frac{d(\delta \overline{V}_{a1})}{dt} + \sum_{k=1}^{3} \frac{\partial R_m}{\partial \omega_k} k \frac{d(\delta \phi_1)}{dt}$$

$$+ \sum_{k=1}^{3} \frac{\partial R_m}{\partial \phi_k} a_k + \sum_{k=1}^{3} \frac{\partial R_m}{\partial \overline{V}_{ak}} b_k = 0 \qquad (3.57)$$

and

$$\sum_{k=1}^{3} k \frac{\partial K_m}{\partial \overline{V}_{ak}} \delta \overline{V}_{a1} - \sum_{k=1}^{3} \frac{\partial R_m}{\partial \omega_k} k \frac{d(\delta \overline{V}_{a1})}{dt} + \sum_{k=1}^{3} \frac{\partial K_m}{\partial \omega_k} k \frac{d(\delta \phi_1)}{dt}$$

$$+ \sum_{k=1}^{3} \frac{\partial K_m}{\partial \phi_k} a_k + \sum_{k=1}^{3} \frac{\partial K_m}{\partial \overline{V}_{ak}} b_k = 0 \quad . \quad (3.58)$$

Since a_1 and b_1 are both zero, the preceding equations for $m = 1$ to 3 consist of seven independent variables. It is possible to solve them

in terms of $d(\delta \overline{V}_{a1})/dt$. Thus

$$\delta \overline{V}_{a1} = \gamma \frac{d(\delta \overline{V}_{a1})}{dt} , \qquad (3.59)$$

where $\gamma = \det_{\overline{M}_A}/\det_{\overline{M}_B}$ and $\overline{M}_A$ is represented by the following matrix:

$$\begin{bmatrix}
\sum\limits_{k=1}^{3} k \dfrac{\partial R_1}{\partial \overline{V}_{ak}} & \dfrac{dR_1}{d\omega_1} & \dfrac{\partial R_1}{\partial \phi_2} & \dfrac{\partial R_1}{\partial \phi_3} & \dfrac{\partial R_1}{\partial \overline{V}_{a2}} & \dfrac{\partial R_1}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k \dfrac{\partial K_1}{\partial \overline{V}_{ak}} & \dfrac{dK_1}{d\omega_1} & \dfrac{\partial K_1}{\partial \phi_2} & \dfrac{\partial K_1}{\partial \phi_3} & \dfrac{\partial K_1}{\partial \overline{V}_{a2}} & \dfrac{\partial K_1}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k \dfrac{\partial R_2}{\partial \overline{V}_{ak}} & \dfrac{dR_2}{d\omega_1} & \dfrac{\partial R_2}{\partial \phi_2} & \dfrac{\partial R_2}{\partial \phi_3} & \dfrac{\partial R_2}{\partial \overline{V}_{a2}} & \dfrac{\partial R_2}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k \dfrac{\partial K_2}{\partial \overline{V}_{ak}} & \dfrac{dK_2}{d\omega_1} & \dfrac{\partial K_2}{\partial \phi_2} & \dfrac{\partial K_3}{\partial \phi_3} & \dfrac{\partial K_2}{\partial \overline{V}_{a2}} & \dfrac{\partial K_2}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k \dfrac{\partial R_3}{\partial \overline{V}_{ak}} & \dfrac{dR_3}{d\omega_1} & \dfrac{\partial R_3}{\partial \phi_2} & \dfrac{\partial R_3}{\partial \phi_3} & \dfrac{\partial R_3}{\partial \overline{V}_{a2}} & \dfrac{\partial R_3}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k \dfrac{\partial K_3}{\partial \overline{V}_{ak}} & \dfrac{dK_3}{d\omega} & \dfrac{\partial K_3}{\partial \phi_2} & \dfrac{\partial K_3}{\partial \phi_3} & \dfrac{\partial K_3}{\partial \overline{V}_{a2}} & \dfrac{\partial K_3}{\partial \overline{V}_{a3}}
\end{bmatrix} ,$$

where $(dR_m/d\omega_1) = \sum k \, (\partial R_m/\partial \omega_k)$ and $(dK_m/d\omega_1) = \sum k \, (\partial K_m/\partial \omega_k)$. Matrix M_B can be obtained by replacing the first column of matrix M_A by the following column vector

$$\left[-\sum_{k=1}^{3} k \frac{\partial K_1}{\partial \omega_k} , \; \sum_{k=1}^{3} k \frac{\partial R_1}{\partial \omega_k} , \; -\sum_{k=1}^{3} k \frac{\partial K_2}{\partial \omega_k} , \; \sum_{k=1}^{3} k \frac{\partial R_2}{\partial \omega_k} , \right.$$
$$\left. -\sum_{k=1}^{3} k \frac{\partial K_3}{\partial \omega_k} , \; \sum_{k=1}^{3} k \frac{\partial R_3}{\partial \omega_k} \right] .$$

The stability of oscillation requires that the $\delta\overline{V}_{ak}$ decrease with time, i.e., $\gamma < 0$. The value of γ is dependent on the mutual effect between the signals, which is not significant as long as the depletion-layer modulation effect is not included in the model used here. The case where the fundamental voltage is relatively high but does not drive the diode into depletion-layer modulation is considered. The harmonic signals have a very small effect on R_1 and K_1. Hence the terms associated with the differentiations of R_1 and K_1 with respect to V_{a2}, V_{a3}, ϕ_2 and ϕ_3 can be neglected and matrix M_A becomes

$$
\begin{bmatrix}
\sum\limits_{k=1}^{3} k\dfrac{\partial R_1}{\partial \overline{V}_{ak}} & \dfrac{dR_1}{d\omega_1} & 0 & 0 & 0 & 0 \\[2em]
\sum\limits_{k=1}^{3} k\dfrac{\partial K_1}{\partial \overline{V}_{ak}} & \dfrac{dK_1}{d\omega_1} & 0 & 0 & 0 & 0 \\[2em]
\sum\limits_{k=1}^{3} k\dfrac{\partial R_2}{\partial \overline{V}_{ak}} & \dfrac{dR_2}{d\omega_1} & \dfrac{\partial R_2}{\partial \phi_2} & \dfrac{\partial R_2}{\partial \phi_3} & \dfrac{\partial R_2}{\partial \overline{V}_{a2}} & \dfrac{\partial R_3}{\partial \overline{V}_{a2}} \\[2em]
\sum\limits_{k=1}^{3} k\dfrac{\partial K_2}{\partial \overline{V}_{ak}} & \dfrac{dK_2}{d\omega_1} & \dfrac{\partial K_2}{\partial \phi_2} & \dfrac{\partial K_2}{\partial \phi_3} & \dfrac{\partial K_2}{\partial \overline{V}_{a2}} & \dfrac{\partial K_2}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k\dfrac{\partial R_3}{\partial \overline{V}_{ak}} & \dfrac{dR_3}{d\omega_1} & \dfrac{\partial R_3}{\partial \phi_2} & \dfrac{\partial R_3}{\partial \phi_3} & \dfrac{\partial R_3}{\partial \overline{V}_{a2}} & \dfrac{\partial R_3}{\partial \overline{V}_{a3}} \\[2em]
\sum\limits_{k=1}^{3} k\dfrac{\partial K_3}{\partial \overline{V}_{ak}} & \dfrac{dK_3}{d\omega_1} & \dfrac{\partial K_3}{\partial \phi_2} & \dfrac{\partial K_3}{\partial \phi_3} & \dfrac{\partial K_3}{\partial \overline{V}_{a2}} & \dfrac{\partial K_3}{\partial \overline{V}_{a3}}
\end{bmatrix}
$$

The same approximation can also be applied to matrix M_B. Then

γ is found to be

$$\gamma = -\frac{\left(\dfrac{dK_1}{d\omega_1}\right)^2 + \left(\dfrac{dR_1}{d\omega_1}\right)^2}{\dfrac{\partial R_1}{\partial \overline{V}_{a1}}\dfrac{dK_1}{d\omega_1} - \dfrac{dR_1}{d\omega_1}\dfrac{\partial K_1}{\partial \overline{V}_{a1}}} \quad . \tag{3.60}$$

Since the numerator in Eq. 3.60 is always positive, this implies that

$$\frac{\partial R_1}{\partial \overline{V}_{a1}}\frac{dK_1}{d\omega_1} - \frac{dR_1}{d\omega_1}\frac{\partial K_1}{\partial \overline{V}_{a1}} > 0 \quad . \tag{3.61}$$

The stability criterion derived here is the same as that for a single-frequency oscillator. When the definitions of R_1 and J_1 are used, the stability criterion becomes

$$\frac{\partial}{\partial \overline{V}_{a1}}\left[\text{Re}\left(\frac{\beta_1}{v_{a1}}\right)\right]\frac{d}{d\omega_1}\,\text{Im}\left(\frac{\beta_1}{v_{a1}} + \frac{X}{\rho_1}\right) - \frac{d}{d\omega_1}\,\text{Re}\left(\frac{X}{\rho_1} + \frac{\beta_1}{v_{a1}}\right)\frac{\partial}{\partial \overline{V}_{a1}}\,\text{Im}\left(\frac{\beta_1}{v_{a1}}\right) \geq 0 \quad . \tag{3.62}$$

This stability criterion states that for a nonlinear device having a neglible effect of harmonic signals on the fundamental signal, the fundamental frequency circuit determines the overall stability of the oscillator. Although it is known that the effect of the harmonic signals on the fundamental signal always exists, the fundamental frequency circuit still plays an important role in the oscillator stability criterion. If the diode is operated under the depletion-layer modulation condition, the stability criterion is not uniquely determined by the fundamental frequency circuit. It is determined by the sign and magnitude of the coupling terms in matrices M_A and M_B.

3.5 Large-Signal Analysis

In this section the performance of the diode at the third harmonic under large-signal operation and different loading conditions is discussed. Also, the series resistance effect is investigated in order to determine the optimum loading condition for operation at the third-harmonic frequency.

3.5.1 Single-Frequency Operation.

In order to calculate the Fourier components of the injected current J_{inj} in the presence of three harmonically related signals, Eq. 3.21 should be expanded in terms of modified Bessel functions of the first kind I_n. Applying the following identity

$$\exp \left[-|v_{am}| \cos (m\omega t + \phi_m) \right] = \sum_{n=-\infty}^{\infty} I_n(-|v_{am}|) \exp (jnm\omega t + n\phi_m)$$

(3.63)

yields the injected current

$$J_{inj} = J_{dc} \left[1 + \sum_{m=1}^{\infty} \left(\frac{\beta_m}{2} \exp jm\omega t + \frac{\beta_m^*}{2} \exp (jm\omega t) \right) \right]$$

$$= J_{co} \exp \left(\sum_{m=1}^{3} |v_{am}| \cos \phi_m \right) \sum_p^{\infty} \sum_q^{\infty} \sum_r^{\infty} I_p(-v_{a1}) I_q(-|v_{a2}|) I_r(-|v_{a3}|)$$

$$\cdot \exp [j(q\phi_2 + r\phi_3)] \exp [j(p + 2q + 3r)\omega t] \quad , \quad (3.64)$$

where $I_n(-|v_{am}|) = -1^n I_n(|v_{am}|)$ and $I_{-n} = I_n$. Equating the terms with the same frequency on both sides of Eq. 3.64 yields

$$J_{dc} = J_{co} \exp \left(\sum_{m=1}^{3} |v_{am}| \cos \phi_m \right) \sum_q^{\infty} \sum_r^{\infty} I_{-2q-3r}(-|v_{a1}|) I_q(-|v_{a2}|)$$

$$\cdot I_r(-|v_{a3}|) \exp [j(q\phi_2 + r\phi_3)] \quad (3.65)$$

and

$$\beta_m = \frac{\sum\limits_{q}\sum\limits_{r}^{\infty}{}^{\infty} I_{m-2q-2r}(-|v_{a1}|) I_q(-|v_{a2}|) I_r(-|v_{a3}|) \exp[j(q\phi_2 + r\phi_3)]}{\sum\limits_{q}\sum\limits_{r} I_{-2q-2r}(-|v_{a1}|) I_q(-|v_{a2}|) I_r(-|v_{a3}|) \exp[j(q\phi_2 + r\phi_3)]} .$$

(3.66)

Since it has been shown that v_{a2} and v_{a3} are small in magnitude, compared to the fundamental voltage v_{a1}, the higher-order terms of the Bessel functions of the first kind become negligible, which leads to simplification of the b_m coefficient. Therefore, for the convenience of calculation, only the terms corresponding to $|p| \leqq 3$, $|q| \leqq 1$ and $|r| \leqq 1$ have been retained. In the following numerical example related to the mutual effects between the harmonics, the fundamental frequency has been chosen to be equal to 23 GHz. By specifying v_{am} and ϕ_m, the diode admittance has been calculated. For investigation of loading effects on the third-harmonic power generation, the Newton-Raphson method was adopted to solve the three-frequency oscillation conditions. The amplitude of V_{am} must be checked out to ensure that it will satisfy the approximation described previously. The diode parameters used in the calculation were the same as those used for the small-signal analysis.

The output power at the fundamental and the Fourier components of the induced current calculated from the analytic model described previously are shown in Figs. 3.3 and 3.4. Also shown in both figures are the results of the computer simulation for the GaAs double-Read diode carried out in Chapter II. At low RF voltages, the results calculated from both the analytic model and computer simulation are in good agreement. At high voltages, the fundamental
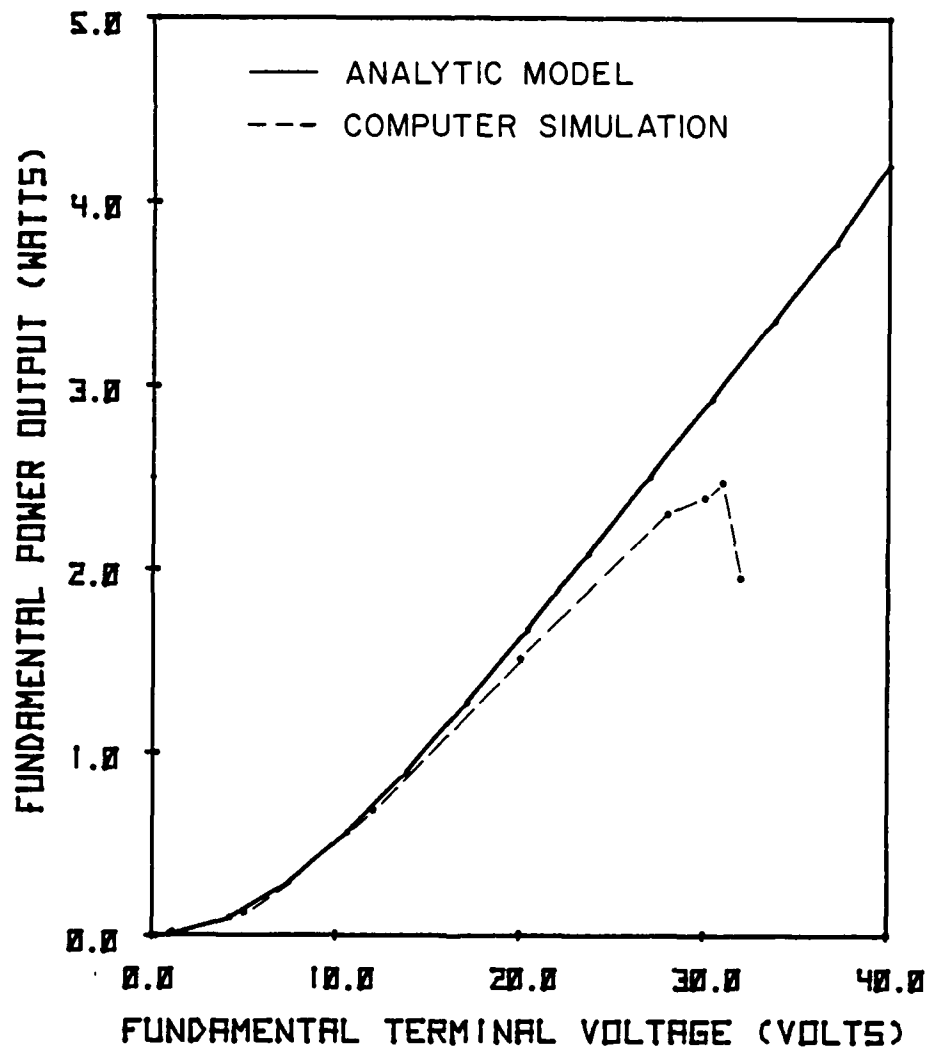
FIG. 3.3 COMPARISON FOR THE FUNDAMENTAL OUTPUT POWER

BETWEEN THE ANALYTIC MODEL AND THE COMPUTER

SIMULATION IN SINGLE-FREQUENCY OPERATION AT

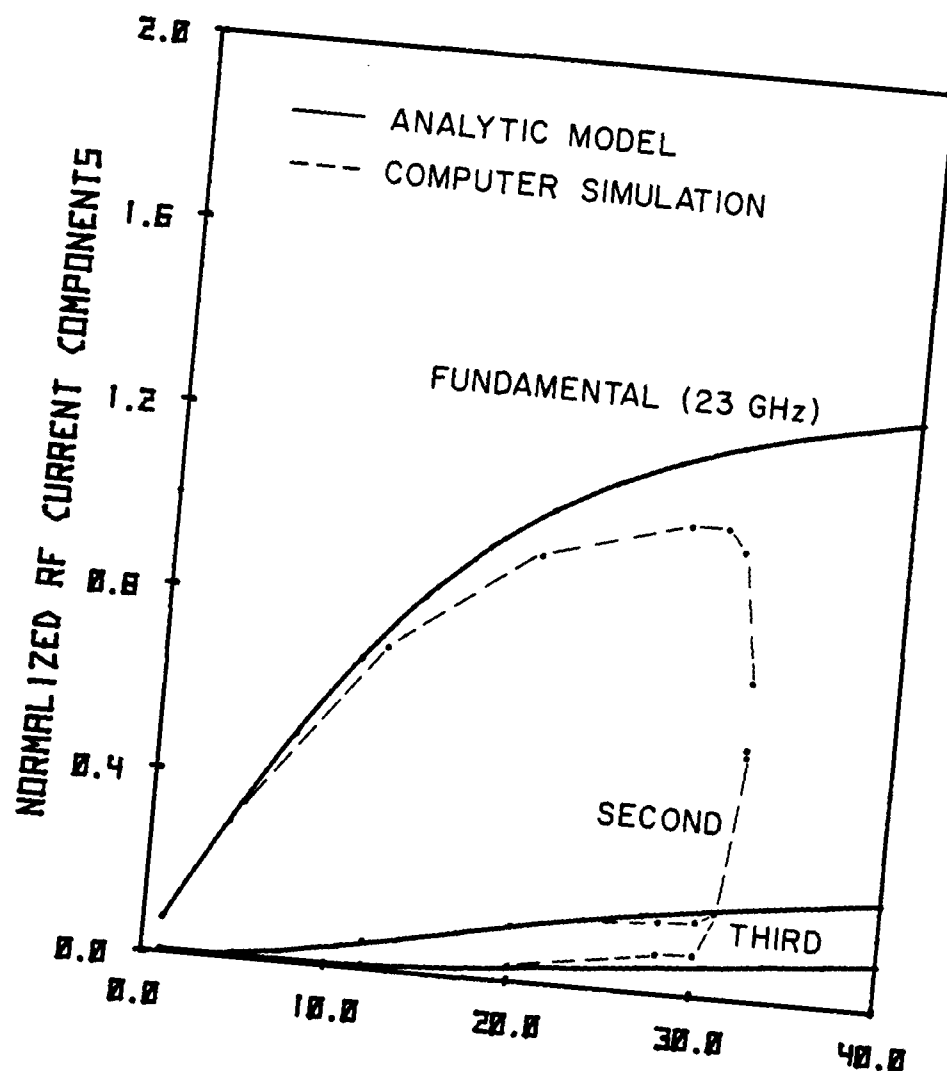f_1 = 23 GHz AND J_{dc} = 1256 A/cm^2.

FIG. 3.4 COMPARISON FOR THE NORMALIZED FUNDAMENTAL AND HARMONIC COMPONENT OF THE INDUCED CURRENT IN SINGLE-FREQUENCY OPERATION AT f_1 = 23 GHz AND J_{dc} = 1256 A/cm^2.

current and power calculated from the analytic model are higher than those obtained from computer simulation. It is known that the analytic model is simplified and does not take into account the back bias and space-charge effects, which tend to retard the build-up of the injected current with increasing RF voltage level. This means that the analytic model somewhat overestimates the fundamental current and power. Also the depletion-layer modulation, which is not easy to incorporate into an analytic model, brings down the fundamental current and power significantly at extremely high RF voltages and causes a large discrepancy between the calculated results of the analytic model and computer simulation.

The harmonic components of the induced current obtained from either the simplified analysis or computer simulation are small in magnitude compared with the fundamental current component. Good agreement in harmonic components between both calculations can be observed until the depletion-layer modulation effect sets in. It can be said that the space-charge and back-bias effects do not degrade seriously the harmonic current generation of the GaAs double-Read diode. If the depletion-layer modulation is negligible, the analytic model·gives fairly good quantitative results for harmonic power calculation. For further investigation of multifrequency operation, the magnitude of the fundamental voltage signal component is assumed to be less than 30 V in order to ensure that the depletion-layer modulation will not occur.

3.5.2 Mutual Interaction Among Harmonic Signals. The interaction among the harmonically related signals will affect the diode admittance and the RF power output at each signal frequency. The
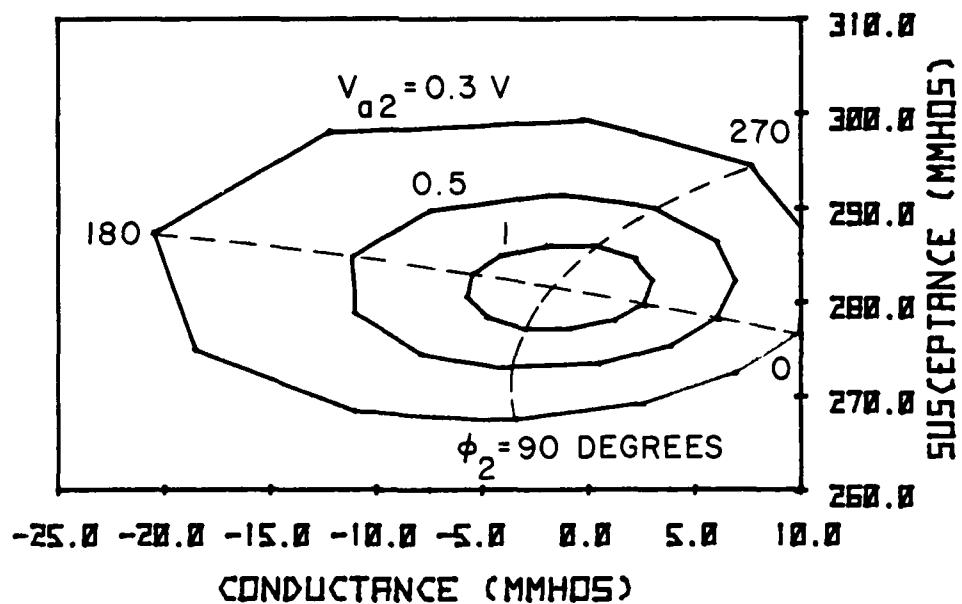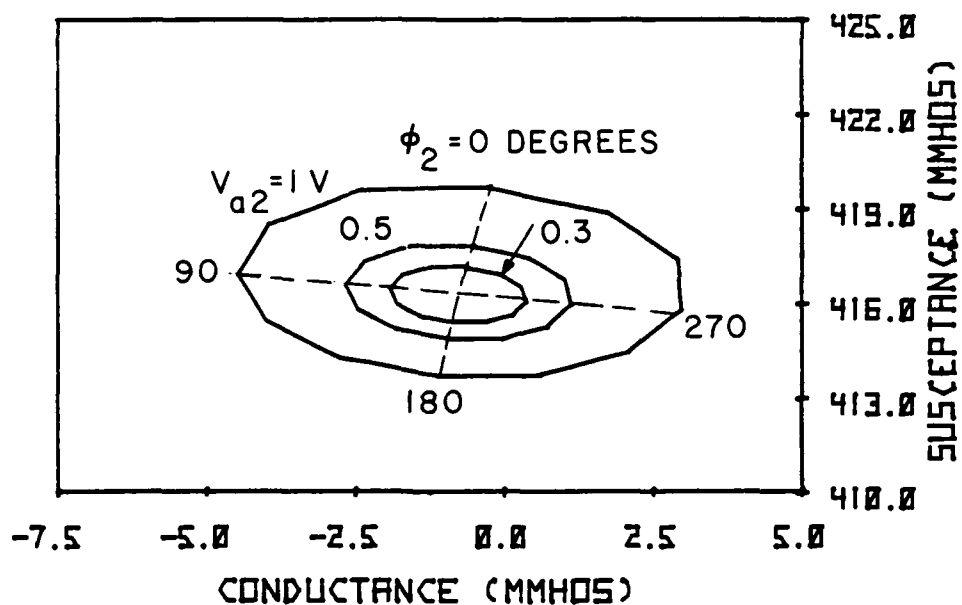
FIG. 3.5 DEVICE HARMONIC ADMITTANCE UNDER THE INFLUENCE OF

SECOND-HARMONIC VOLTAGE FOR V_{a1} = 3.5 V, V_{a3} = 0.375 V

AND ϕ_3 = 0 DEGREES AT f_1 = 23 GHz.

achievable admittance level is important for the design of an oscillator. The interaction among harmonics can be qualitatively understood by the fact that the change in the RF voltage waveform across the avalanche region due to the presence of the harmonic voltage will modify the shape of the injected current waveform. Hence, the harmonic current content in the injected current is subject to modulation with the harmonic voltage. According to Eq. 3.66, the effect of harmonic voltage on the harmonic current is dependent on not only its phase angle but also on its normalized amplitude. In other words, a higher-order harmonic voltage has less effect on the harmonic current generation of the diode. The presence of a low-order harmonic voltage seems to be useful for improving the high-order harmonic current generation. The improvement depends on the relative phase angle and amplitude of the additional harmonic voltage. The device admittance in the presence of harmonic signals is discussed next.

First, the effect of the second-harmonic voltage on the device harmonic admittance is discussed. Figure 3.5 shows the device harmonic admittance at V_{a1} = 3.5 V, V_{a3} = 0.375 V and ϕ_3 = 0 degrees. As the second-harmonic voltage phase angle ϕ_2 varies from 0 to 360 degrees, the locus of the second-harmonic admittance on the G-B plane moves in a clockwise direction and forms a loop. For each V_{a2}, the second-harmonic conductance reaches its most negative value around 180 degrees and its most positive value around 0 degrees. This indicates that ϕ_2 should be chosen close to 180 degrees in order to maintain the diode in the active mode. As the second-harmonic voltage decreases, the admittance loop becomes larger in size. This property guarantees the second-harmonic power generation for

any load condition with a positive circuit resistance at the
second-harmonic circuit, as long as the oscillator can maintain
the fundamental signal at a certain level.

The influence of the second-harmonic voltage on the third-
harmonic admittance can also be seen from the characteristics shown
in Fig. 3.5. The locus of the third-harmonic admittance on the G-B
plane moves in a counterclockwise direction as ϕ_2 increases from 0 to
360 degrees. It is clear from the figure that a higher second-harmonic
voltage causes a significant variation in the third-harmonic admittance.
This admittance goes to its most negative value at ϕ_2 close to 90
degrees. In other words, a proper choice of ϕ_2 can improve the third-
harmonic admittance to some degree and also enhances the third-
harmonic power since the power is equal to $- (1/2)G_{d3}V_3^2$ (V_3 is the
terminal third-harmonic voltage which is proportional to V_{a3}). When
ϕ_3 approaches 90 degrees, as shown in Fig. 3.6, the negative third-
harmonic conductance is enhanced and reaches its highest value around
$\phi_2 = 180$ degrees. However, the variation in the third-harmonic
admittance with voltage V_{a2} is reduced. This means that the interaction
between the harmonic signals is not as strong as in the previous case.

The loci of the second-harmonic admittance on the G-B plane
have a small variation due to the increase of the third-harmonic
voltage phase angle compared with those in the previous case. It
should also be mentioned that the fundamental admittance is subjected
to a small change when the harmonic voltage is varied. This change
becomes much smaller for a smaller second-harmonic voltage.

The effects of the third-harmonic voltage on the harmonic
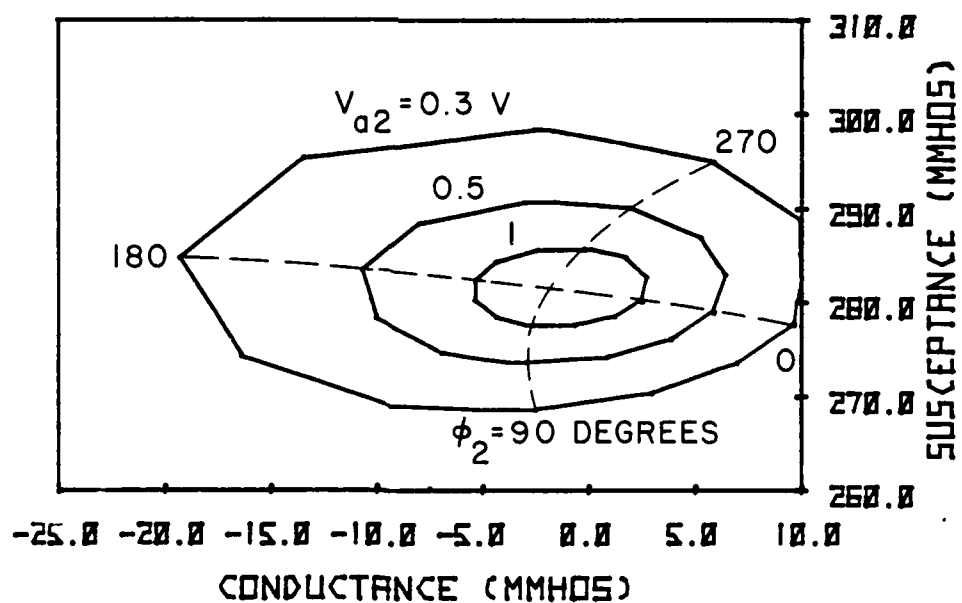admittance is shown in Figs. 3.7 and 3.8 for $V_{a1} = 3.5$ V, $V_{a2} = 0.5$ V
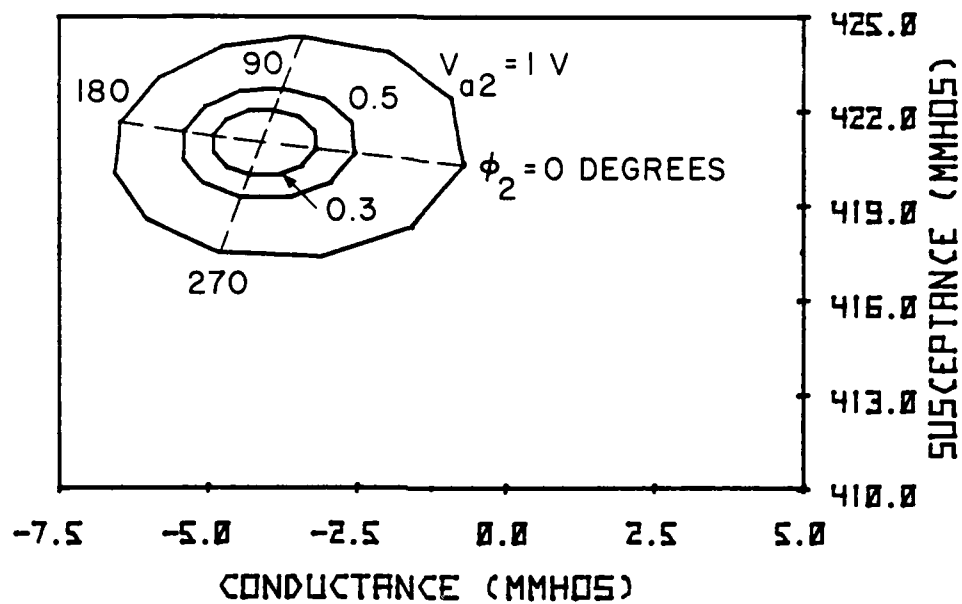
FIG. 3.6 DEVICE HARMONIC ADMITTANCE UNDER THE INFLUENCE OF

SECOND-HARMONIC VOLTAGE FOR V_{a1} = 3.5 V, V_{a3} = 0.375 V

AND ϕ_3 = 90 DEGREES AT f_1 = 23 GHz.
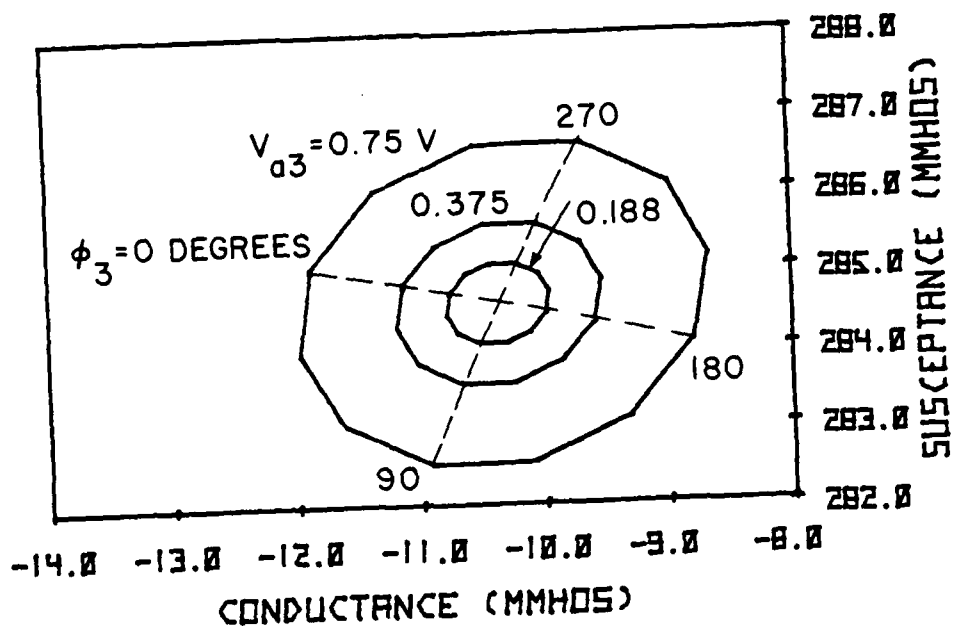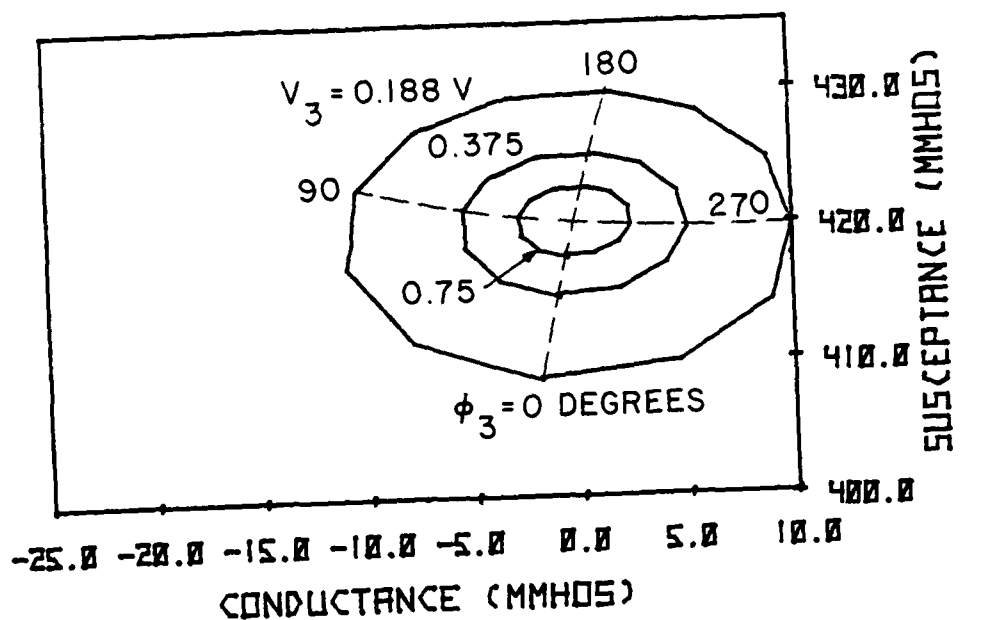
FIG. 3.7 HARMONIC ADMITTANCE UNDER THE INFLUENCE OF THIRD-

HARMONIC VOLTAGE FOR V_{a1} = 3.5 V, V_{a2} = 0.5 V AND

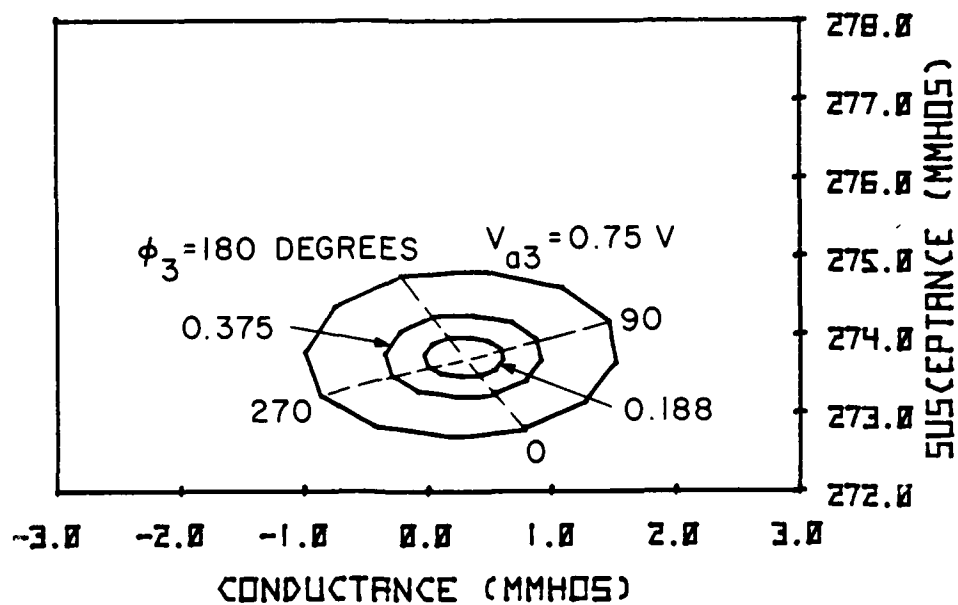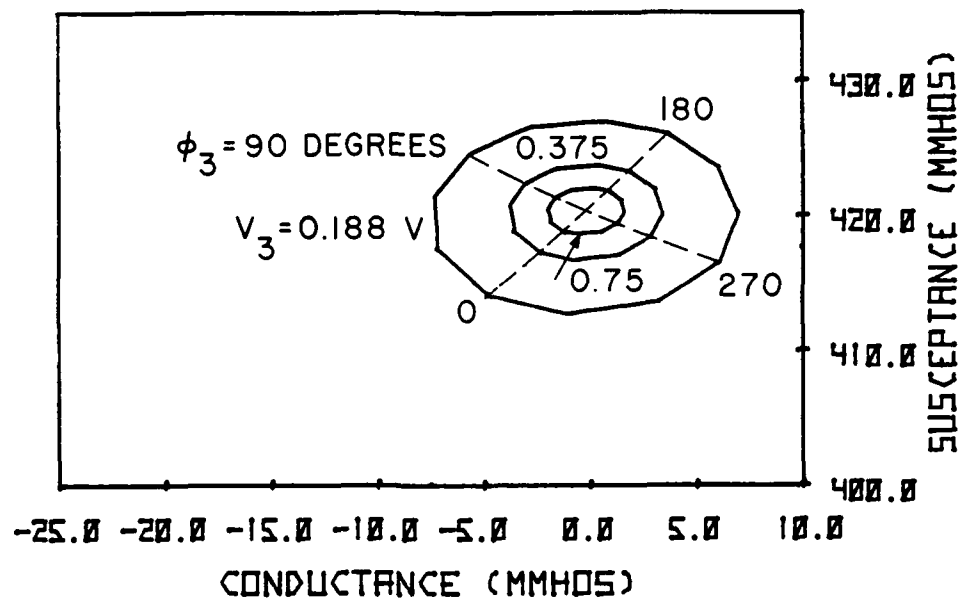ϕ_2 = 180 DEGREES AT f_1 = 23 GHz.

-247-

FIG. 3.8 DEVICE HARMONIC ADMITTANCE UNDER THE INFLUENCE OF THIRD-
HARMONIC VOLTAGE FOR V_{a1} = 3.5 V, V_{a2} = 0.5 V AND ϕ_2 =
60 DEGREES AT f_1 = 23 GHz.

and ϕ_2 = 180 and 60 degrees, respectively. It can be seen in Fig. 3.7 that for ϕ_2 = 180 degrees, the locus of the third-harmonic on the G-B plane moves in the clockwise direction as ϕ_3 increases from 0 to 360 degrees, but the second-harmonic admittance locus moves in the opposite direction. A decrease in the third-harmonic voltage amplitude will enlarge the third-harmonic admittance loop. In comparison with the previous two figures it can be found that the third-harmonic voltage has a smaller effect on the second-harmonic than vice versa. The reason is related to the inverse dependence of the normalized harmonic voltage across the avalanche region on the harmonic number. It can be found that for each V_{a3}, the optimum third-harmonic voltage phase angle to achieve the maximum negative third-harmonic conductance is approximately 90 degrees.

As ϕ_2 is changed to 60 degrees, a significant change in both harmonic admittances can be seen from Fig. 3.8. The mutual influence between the harmonics is reduced in strength in this case. The second-harmonic conductance goes to zero at the two different values of ϕ_3 close to 180 and 300 degrees, respectively. The corresponding negative third-harmonic conductance is less than its maximum value. This will yield small third-harmonic power generation. In other words, a reactive loading at the second harmonic is not necessarily good for an efficient third-harmonic power generation. In addition, when the negative third-harmonic conductance reaches its maximum value, the second-harmonic conductance may become positive. Hence, active mode operation may not be maintained.

3.5.3 Reactive and Nonreactive Loading for the Second-Harmonic Signals. In the analysis presented here for a third-harmonic power

generation from a self-oscillating IMPATT diode, the second-harmonic

signal will be treated as an idler. Proper design of the second-

harmonic signal can ensure optimum conditions for third-harmonic

power generation. In order to consider the effects of the second-

harmonic circuit on the third-harmonic power generation, ϕ_3 is

kept constant at 90 degrees since this results in a maximum negative

third-harmonic conductance. The power calculated from this condition

is believed to be close to the maximum value. In the following cal-

culation, V_{a3} is chosen to be 0.1 and 0.375 V. It is noted that for

these values of V_{a3}, the negative third-harmonic resistance is

usually small in magnitude.

Reactive loading at the second harmonic can be accomplished

by adjusting ϕ_2 in such a way that the second-harmonic conductance

is zero at a given value of V_{am}. It is apparent that the condition

for the zero second-harmonic conductance occurs at two different values

of ϕ_2. The value of the corresponding ϕ_2 varies from 30 to 90

degrees for one condition and from 210 to 300 degrees for the other

condition. This difference in values creates the difference in the

third-harmonic power and impedance level between the two conditions.

As shown in Fig. 3.9, the third-harmonic power corresponding to the

first condition (the solid line in the figure) is lower than that

corresponding to the second condition (the dashed line) and is very

sensitive with respect to the second-harmonic voltage. The power

for the second condition is not sensitive to V_{a2} variation up to the

level of V_{a2} equal to 1 V. It is worth mentioning that the impedance

level for the first condition is slightly lower than that for the

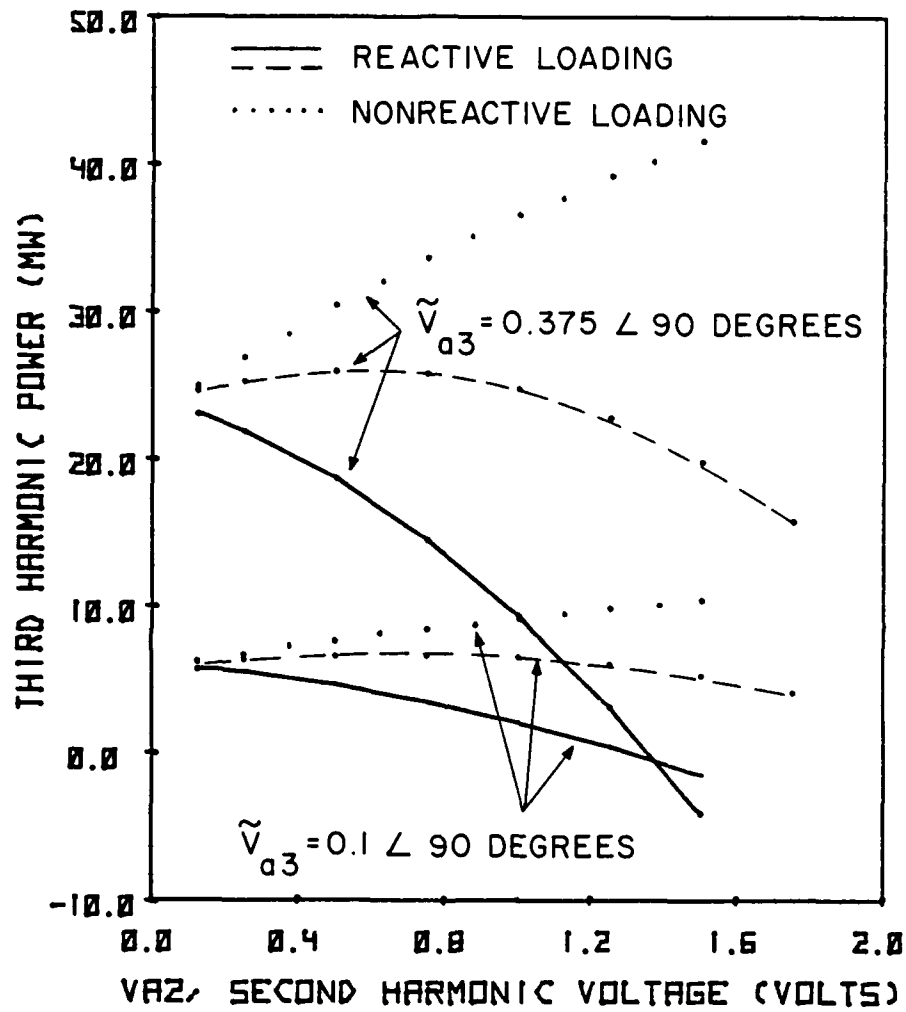second condition. As long as the reactive loading at the second

FIG. 3.9   THIRD-HARMONIC POWER OUTPUT FOR REACTIVE AND

NONREACTIVE LOADING AT THE SECOND HARMONIC.

$(f_1 = 23\ GHz)$

harmonic is concerned, it is better to operate the diode at the

second condition. The nonreactive loading considered here is

achieved by adjusting the value of ϕ_2 such that the third-harmonic

power is maximized at a given value of V_{am}. This condition is

usually achieved along with a level of second-harmonic power genera-

tion. The corresponding ϕ_2 is around 180 degrees. The third-

harmonic power is always higher than that of the reactive loading

condition and shows an increase with V_{a2}. In addition to the power,

the third harmonic impedance level for this loading is

slightly higher than that of the previous case. Hence, in terms of

the power and third-harmonic impedance level, the nonreactive loading

condition is more advantageous than the reactive loading condition.

It is noted that the difference in the power between both loading

conditions becomes small at small V_{a2}. It is obvious because

interaction between the harmonics is small at small V_{a2}.

It can be concluded that for optimum third-harmonic power gen-

eration, the IMPATT diode should be nonreactively loaded at the

second harmonic, and the second-harmonic voltage amplitude should

be kept as high as possible in order to enhance the third-harmonic

power generation. Since the model does not include the effects of

depletion-layer modulation, reactive loading at the fundamental is

physically impossible to attain except by adding a series resistance

which causes an undesirable effect in the RF output.

3.5.4 Optimum Loading for Third-Harmonic Power Generation
Including the Effect of Series Resistance. Circuit realization is

important for the design of an IMPATT diode oscillator to generate

third-harmonic power. The operating point should be chosen in such

a way that the corresponding negative device resistance at each signal is high in magnitude. A high negative third-harmonic resistance can be achieved with a small third-harmonic voltage amplitude because of small third-harmonic current amplitude. This, in turn, will reduce the third-harmonic power generation. In addition to this, the series resistance, which always exists in a practical diode, can introduce further degradation of the diode third-harmonic power generation capability. Hence, the achievable third-harmonic power is limited by the circuit realization and the series resistance of the diode. The optimum loading condition including these is discussed next.

In order to determine the diode power performance for a given load circuit, the voltage V_{am} across the avalanche region should be solved from the oscillation condition given by Eq. 3.15. The equivalent load circuit considered here consists of the inductance L_m in series with the resistance R_{cm}. There are a total of six circuit elements that must be adjusted properly in order to obtain an optimum power operating condition. Since the device impedance at the fundamental frequency remains unchanged at small harmonic voltages, the fundamental inductance and load resistance can be assumed to be constant without loss of generality. For the convenience of calculation, the inductances (L_2 and L_3) are also assumed unchanged. The third-harmonic power is calculated by adjusting only the load resistances R_{c2} and R_{c3}. If the choice of L_2 and L_3 is proper, the calculated third-harmonic power can be close to its maximum value. These four circuit elements, i.e., L_1, L_2, L_3 and R_{c1} have been determined from the device impedance at $V_{a_1} = 3.5$ V, $V_{a_2} = 0.125$ V,

ϕ_2 = 188.5 degrees, V_{a3} = 0.1 V and ϕ_3 = 90 degrees, and the values

of these elements are L_1 = 50.8 pH, L_2 = 12.057 pH, L_3 = 5.405 pH

and R_{c1} = 0.34348 Ω.

The case of R_s = 0 Ω is considered first. The calculated

third-harmonic power for various R_{c2} and R_{c3} is shown in Fig. 3.10.

The third-harmonic power indicates a monotonic decrease with an

increase of R_{c3} due to the reduction in magnitude of V_{a3}. The

operating terminal voltage V_3 varies from 1.5 to 0.055 V for R_{c3}

between 0.055 and 2 Ω. Increasing V_{a2} by reducing R_{c2} can enhance

the third-harmonic power. An average increase of 1.3 dB was

observed for R_{c2} changing from 1 to 0.2 Ω. There is also little

change of power at the fundamental frequency if R_{c2} and R_{c3} are

varying. The power at the fundamental was approximately 3 W. If

the minimum realizable circuit resistance is 0.2 Ω, then the

optimum third-harmonic power for R_s = 0 Ω is 4.06 mW (6.08 dBm),

which is much smaller than that predicted from the calculation

obtained from computer simulation. The discrepancy is due to

neglecting the depletion-layer modulation effect.

Now, the effects of the series resistance R_s are taken into

account with no change of the circuit element values. The values

of the series resistance were chosen to be 0.1, 0.15 and 0.2 Ω.

The presence of the series resistance R_s will lower the magnitude

of the operating fundamental voltage. As a result, the harmonic

current is reduced and the interaction effect among signals becomes

weak. In addition, only the part of the useful power that is

proportional to $R_{c3}/(R_s + R_{c3})$ is delivered to the load. If R_{c3}

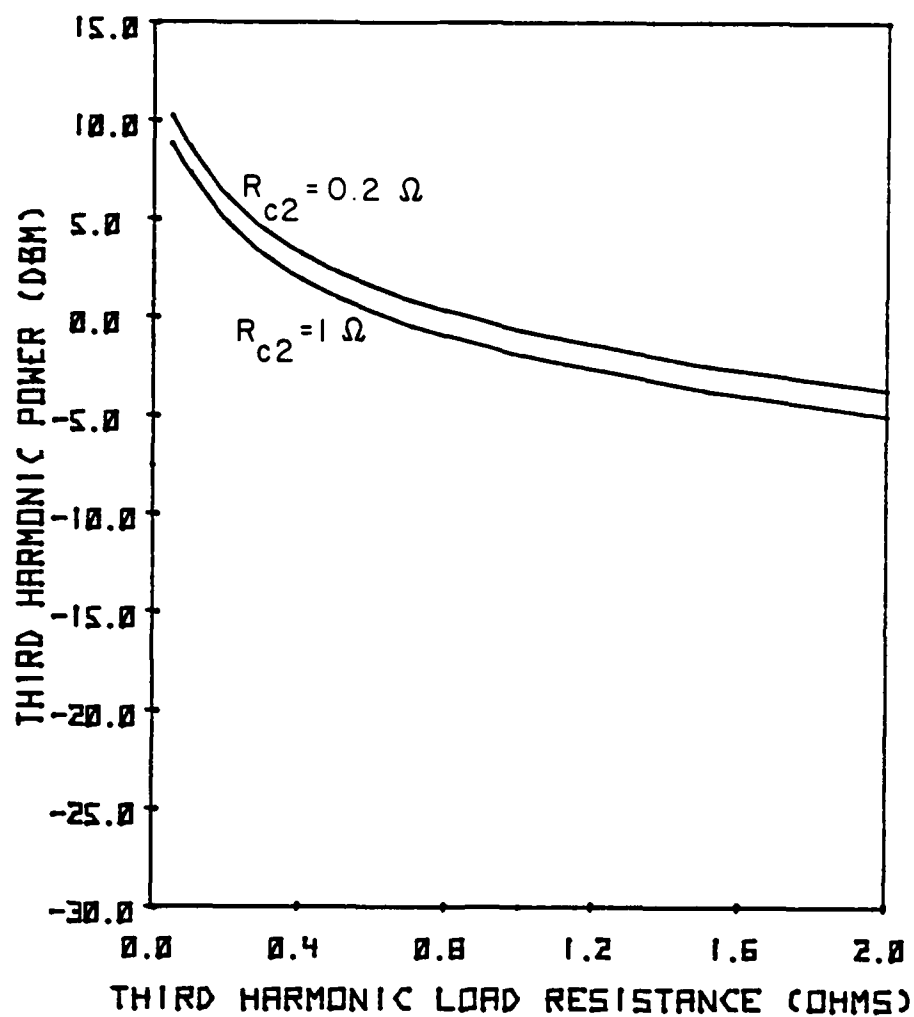is much smaller than R_s, then most of the useful power will dissipate

FIG. 3.10 OUTPUT POWER AT THE THIRD-HARMONIC FREQUENCY (~ 69 GHz)

OBTAINED AT R_s = 0 Ω FOR DIFFERENT HARMONIC LOAD

RESISTANCES. (R_{c2} = 0.2 AND 1 Ω AND R_{c3} = 0.1 TO 2 Ω)

in the series resistance and the actual output power will be reduced
significantly. For R_{c3} much larger than R_s, the series resistance
will absorb very little of the useful power. Figure 3.11 shows the
third-harmonic power obtained at $R_{c2} = 0.2 \ \Omega$ for different values of
R_s. The third-harmonic power has its maximum between $R_{c3} = 0.1$ and
$0.2 \ \Omega$. The peak value of the third-harmonic power drops from 0.48
mW (- 3.18 dBm) at $R_s = 0.1 \ \Omega$ to 17 μW (- 17.5 dBm) at $R_s = 0.2 \ \Omega$.
The corresponding fundamental frequency has 1-percent variation around
23 GHz, but the fundamental power is reduced from 1.35 to 0.417 W.
Similarly, the operating fundamental voltage shifts from 20.7 to
11.8 V. The shift in fundamental voltage is responsible for the drop
of the third-harmonic power. If the fundamental voltage remains un-
changed, the third-harmonic power is degraded approximately by the
factor of $R_{c3}/(R_s + R_{c3})$. When the total resistance $R_s + R_{c1}$ is
kept equal to 0.34348 Ω, the terminal voltage V_1 can be maintained
at 30.8 V (or equivalently, $V_{a1} = 3.5$ V). The output power cal-
culated from the analytic model is shown in Fig. 3.12. The results
obtained indicate that there is some improvement in the third-harmonic
power generated. When reactive loading at the fundamental is con-
sidered with $R_{c1} = 0 \ \Omega$ and $R_s = 0.34348 \ \Omega$, without changing the
inductances (L_1, L_2 and L_3 are the same as before), the calculated
third-harmonic output power obtained is shown in Fig. 3.12. Com-
pared with Fig. 3.11, an observable improvement in the third-harmonic
power can be noted. The highest third-harmonic power at this condition
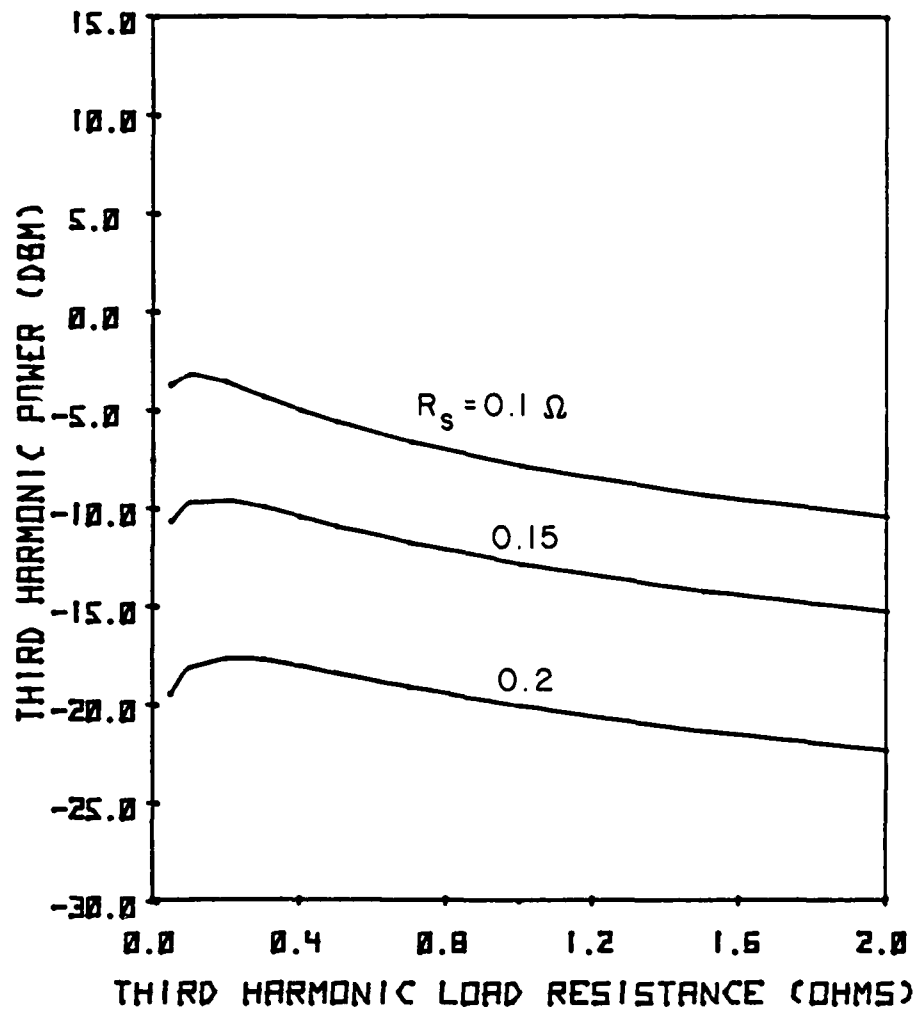is 0.487 mW with $R_{c3} = 0.4 \ \Omega$.

FIG. 3.11 THE EFFECT OF SERIES RESISTANCE ON THIRD-HARMONIC POWER
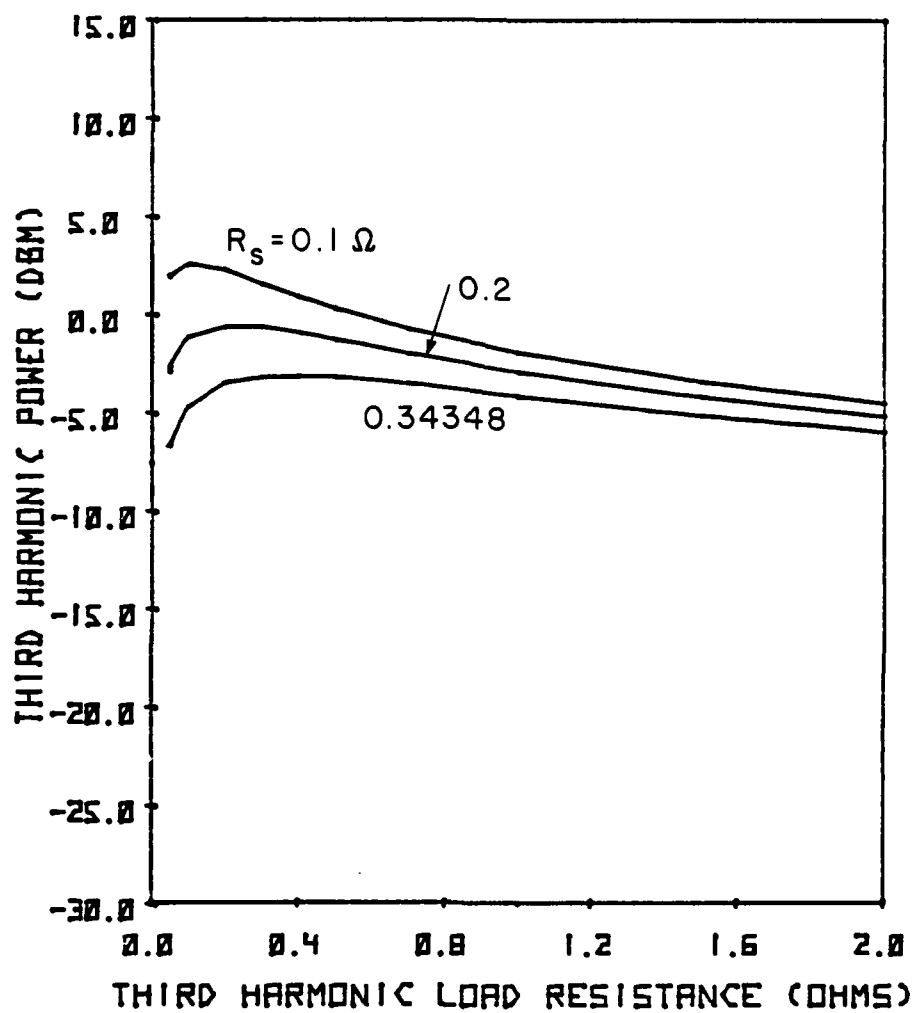
OUTPUT AT R_{c2} = 0.2 Ω.

FIG. 3.12 THIRD-HARMONIC POWER OUTPUT FOR $R_s + R_{c1} = 0.3438 \ \Omega$.

3.6 Conclusions

The calculations using an analytic model for determining the third-harmonic output power P_3 from the IMPATT diode under ideal conditions ($R_s = 0 \ \Omega$) were presented and compared with the calculated values of P_3 obtained from computer simulation. It can be concluded that the depletion-layer modulation is primarily involved in the harmonic diode operation and high harmonic power generation. The calculations have indicated that the presence of a second-harmonic signal can improve the third-harmonic power generation, but this improvement is not very significant. In order to enhance the third-harmonic power generation, the diode should operate at a high level of fundamental voltage. However, the presence of series resistance reduces significantly the fundamental voltage and, therefore, the third-harmonic current is also reduced. Consequently, the third-harmonic power drops to a very small value. It can be concluded that the series resistance should be kept as small as possible to preserve the high level of third-harmonic power generation.

CHAPTER IV

MEASUREMENT OF HARMONIC POWER GENERATION IN IMPATT DIODES

4.1 Introduction

The importance of harmonic operation of an IMPATT diode oscillator has been recognized since its invention. Most of the work on harmonic operation was oriented toward improving the RF power at the fundamental frequency employing the harmonic tuning effect. Several experimental results related to the power generation at harmonic frequencies have also been reported. Using a Harkless oscillator circuit (i.e., Kurokawa oscillator circuit), Allen et al.[94] obtained second-harmonic power of 1 mW and fundamental power of 100 mW at a fundamental frequency of 7.8 GHz. Ohmori et al.[95] obtained second-harmonic power of 0.8 mW and fundamental power of 9 mW at f_1 = 22.5 GHz. These results have been extrapolated from the figures published in References 94 and 95. Bowman and Muller[96] obtained P_2 = 1 mW at f_2 = 140 GHz and P_1 = 160 mW at f_1 = 68 GHz for a Si diode. Birch[97] reported P_3 = 4.5 μW, P_2 = 0.5 mW and P_1 = 20 mW at f_1 = 100 GHz. All of these results indicate that the power generated at harmonic frequencies is at least 10 dB below the level of the fundamental power. The purpose of this study was to investigate the possibility of RF power generation from Si and GaAs diodes under the pulsed mode operating condition, to design a practical oscillator circuit for harmonic power generation, and to compare the experimental results with those obtained from computer simulation. The Harkless-type oscillator was designed for

measuremei.t of the RF power generation from IMPATT diodes operated at a single frequency. For measurement of harmonic power, two- and three-waveguide oscillator circuits were designed in order to produce an independent tuning for each harmonically related signal.

4.2 C-V Characteristics of the Diode Under Test

A C-V profiling technique was applied to packaged Si and GaAs diodes in order to determine the diode doping profile. This is important information to help establish the most suitable diode oscillator circuit for harmonic signal operation. The basic equation relating a diode doping profile to the measured C-V data is given by[98]

$$N_{eff} = \frac{N_D(x_n)N_A(x_p)}{N_D(x_n) + N_A(x_p)} = \frac{2}{q\epsilon A^2} \frac{dV}{d\left(\frac{1}{[C(V) - C_p]^2}\right)} \tag{4.1}$$

and

$$C(V) - C_p = \frac{\epsilon A}{w} = \frac{\epsilon A}{x_n + x_p} , \tag{4.2}$$

where x_n and x_p are the positions of the depletion layer edges in the n- and p-sides of the diode and C_p is the package capacitance. For a uniformly dored structure, the C-V profiling technique employing Shockley's depletion layer approximation can evaluate accurately the doping concentration for the one-sided diode and the effective doping concentration for a double-sided diode. However, this technique gives poor accuracy within the region where the doping changes rapidly.

In order to determine the effective doping profile, the diode diameter must be measured. The GaAs diodes used have four-mesa

structures and each mesa has a diameter of 70 μm to approximately 72 μm. The Si diodes used have single-mesa structures and the mesa diameter is approximately 88.4 μm. The package capacitance is 0.45 pF for the GaAs diodes and 0.18 pF for the Si diodes. This information yields the effective doping profile along with the C-V characteristics that are plotted in Fig. 4.1. It has been observed that, under the presence of a small and finite value of conduction current at the point of junction breakdown and also the forward bias conditions, the capacitance meter used was not suffi-ciently accurate. The calculations of effective doping profile showed that the Si diode has a single drift uniform doping structure with an average doping concentration of approximately 6×10^{16} cm^{-3}, an average diode length of approximately 0.8 μm, and is nonpunch through with a breakdown voltage of approximately 28 V. The measurements obtained showed that the GaAs diode is a double-Read-type structure with a length of approximately 1.82 μm and is punched through at a breakdown voltage of 23 V. The doping concentration of the GaAs diode in each region could not be determined exactly from this C-V measurement.

4.3 Measurement of RF Power Generation in Single-Frequency

Operation

A Harkless-type oscillator circuit was used for power measurement at the fundamental frequency. The oscillator circuit construction and measurement setup are shown in Fig. 4.2. The circuit consists of a TEM-type coaxial line coupled to a rectangular waveguide (WR-42). The diode is placed at the bottom section of the coaxial line shown in Fig. 4.2a. The opposite end of the coaxial line has dc isolation,
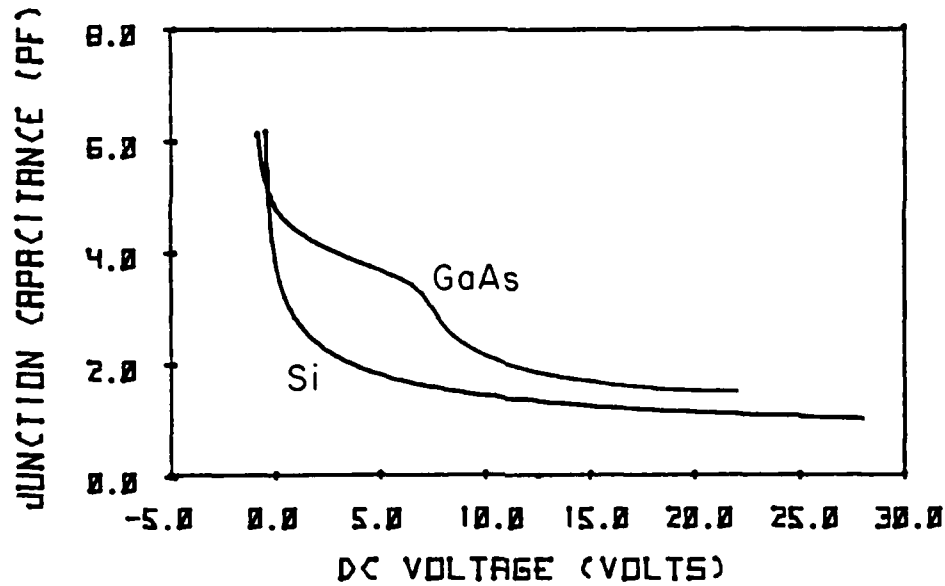
(a)
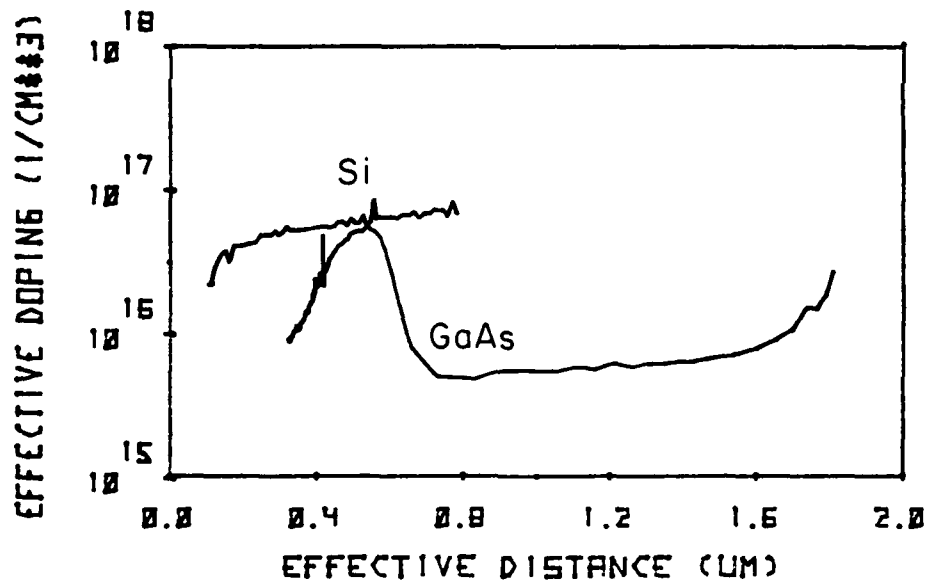
(b)

FIG. 4.1 (a) MEASURED C-V DATA FOR GaAs AND Si IMPATT DIODES

AND (b) CALCULATED DOPING PROFILES FOR GaAs AND Si
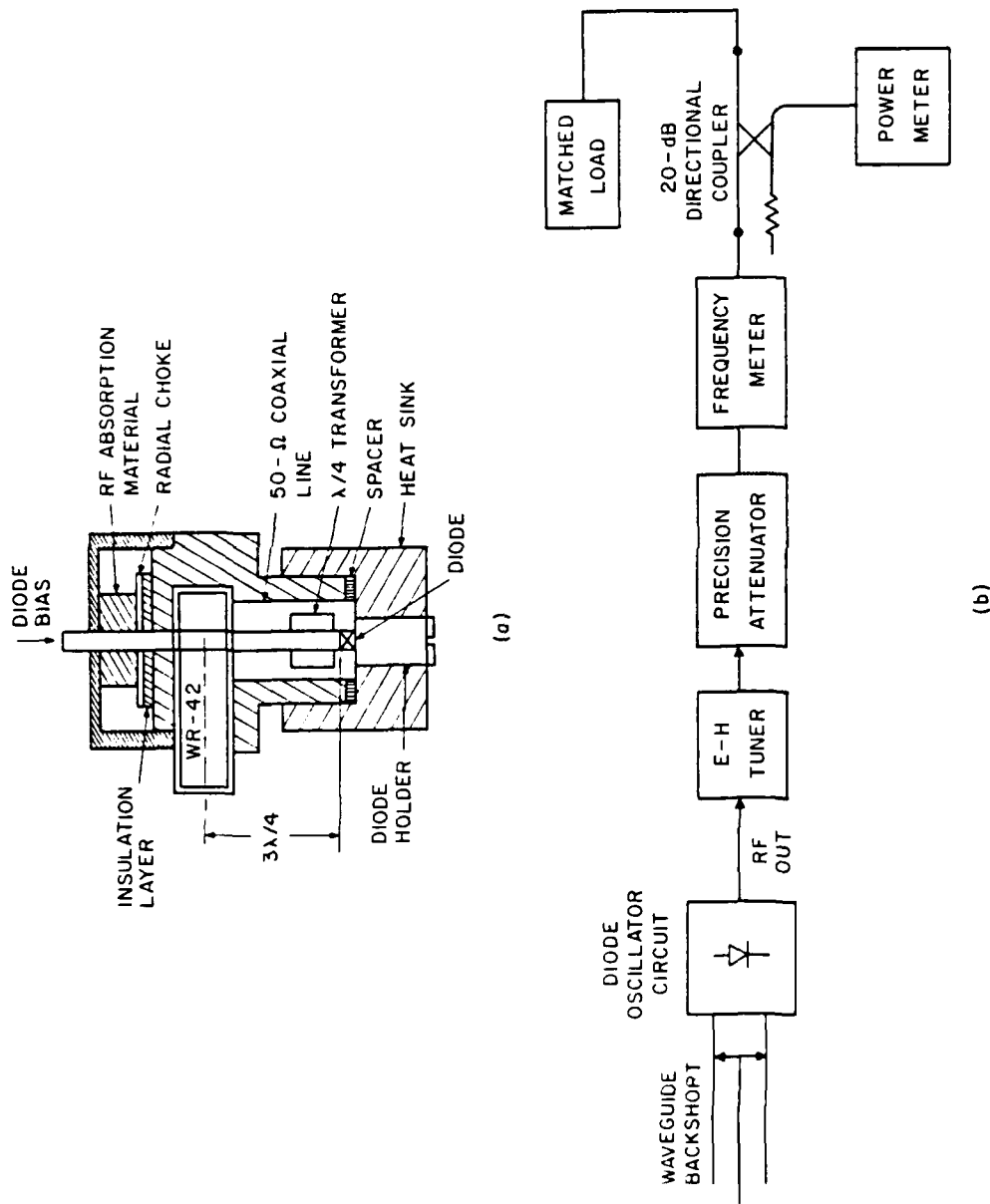
IMAPTT DIODES.

FIG. 1.2 (a) WAVEGUIDE CIRCUIT STRUCTURE FOR SINGLE-FREQUENCY OPERATION AND (b) BLOCK DIAGRAM OF
MEASUREMENT SETUP FOR SINGLE-FREQUENCY OPERATION.

but exhibits a short circuit for the RF signal. The RF absorption
material is used to suppress any possible instability at low fre-
quencies as well as any possible RF leakage. A waveguide backshort
terminates one of the waveguide ports for the purpose of frequency
tuning. The E-H tuner is used at the waveguide output for matching
of the oscillator to the external load. The diode is placed at a
distance of approximately three-quarter wavelength measured from the
waveguide main axis. The diode bias is provided through the center
conductor of the coaxial line section. The quarter-wavelength trans-
former and spacer are replacable components of the circuit which helps
to accommodate the circuit adjustment for a required impedance level
presented by the diode.

The equivalent circuit for the coaxial-waveguide junction, which
constitutes a major part of the oscillator, was studied by many
authors.[99-101] On this basis, the equivalent circuit elements are
usually expressed in terms of the sums of infinite series related to
the dimensions of the waveguide junction circuit. Here, for simplic-
ity, an approximate equation for the circuit input resistance looking
from the coaxial line port to the waveguide has been derived assuming
that the RF current distribution in the center conductor of the
coaxial line is an impulse.[101] The input resistance R_{in} associated
with the only propagating mode (TE_{10}) is given by

$$R_{in} = \frac{2bZ_w}{a} \sin^2\left(\frac{\pi c}{a}\right) \sin(\beta\ell)\left(\frac{\tan(kb)}{kb}\right)^2 , \qquad (4.3)$$

where

$$Z_w = \frac{k}{\beta}\left(\frac{\mu_o}{\epsilon_o}\right)^{1/2} , \qquad (4.4)$$

k and β are wave numbers for the TEM and TE_{10} modes, respectively;

a and b are the width and height of the waveguide, respectively;

c and ℓ are the distances measured from the center conductor of the coaxial line to the waveguide side wall and the backshort, respectively; and ϵ_o and μ_o are the permittivity and permeability of vacuum, respectively. The preceding expression indicates that the input resistance R_{in} strongly depends on the position of the center conductor of the coaxial line relative to the waveguide side wall and waveguide height. In the oscillator circuit used, the center conductor is shifted close to the waveguide side wall in order to make the circuit input resistance presented close to the low impedance of an IMPATT diode.

The GaAs and Si diodes were measured in the pulsed mode of operation. A pulse width of 1 µs with a duty cycle of 10 percent was applied. By adjusting the diameter of the quarter-wavelength transformer and the thickness of the spacer, the maximum RF peak power measured for each quarter-wavelength transformer is indicated in Fig. 4.3. The power sensor (thermistor) used was able to detect not only the power of the fundamental frequency but also the power at the harmonic frequencies generated by the oscillator. The actual power at the fundamental frequency was less than that indicated in Fig. 4.3. However, the transforming section was not exactly a quarter wavelength at the harmonic frequencies so the output power due to the harmonic signals was negligibly small.

The maximum fundamental power of the GaAs diode was 256 mW for a 5-Ω transformer at f_1 = 26.51 GHz and I_p (pulsed current amplitude) = 310 mA. The Si diode generated a maximum fundamental
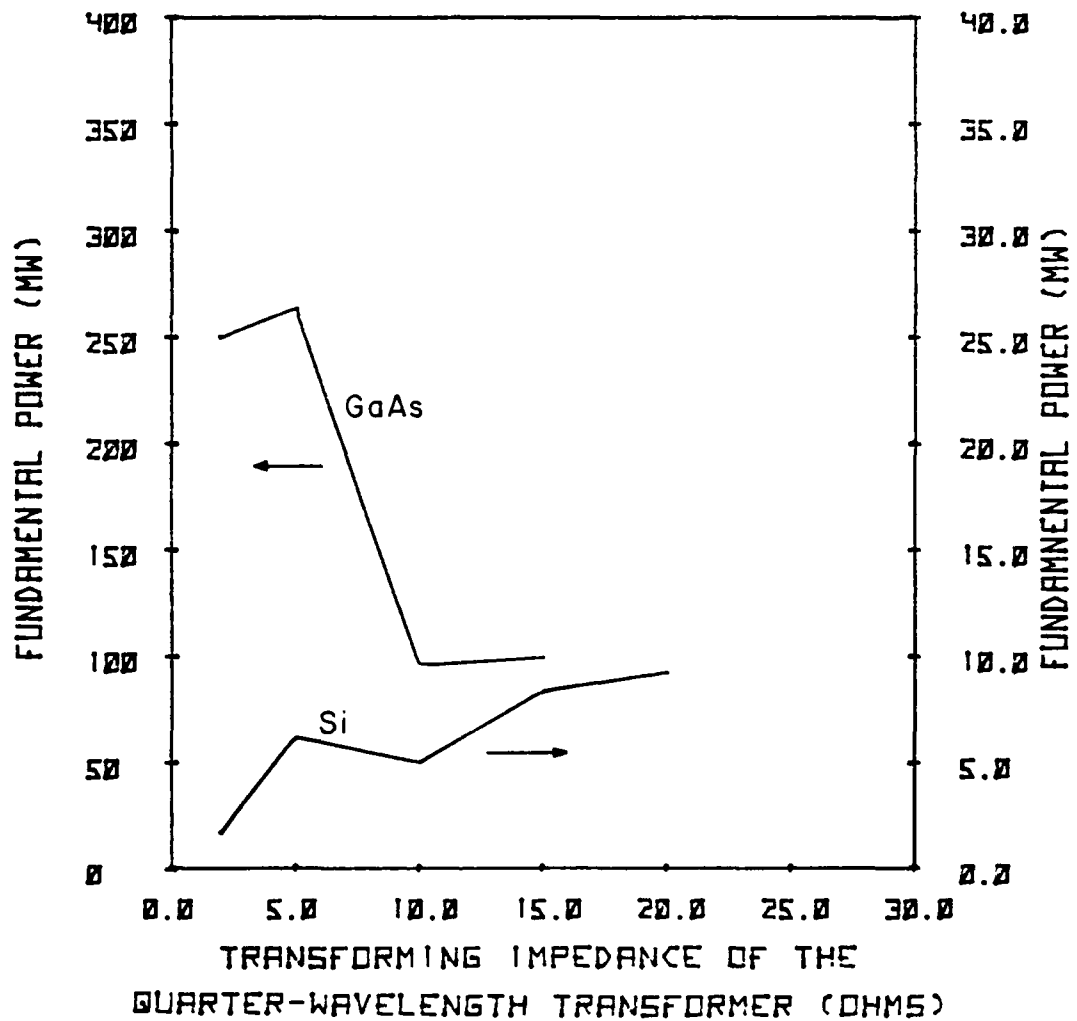
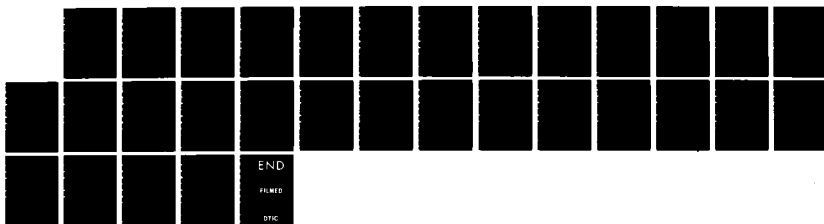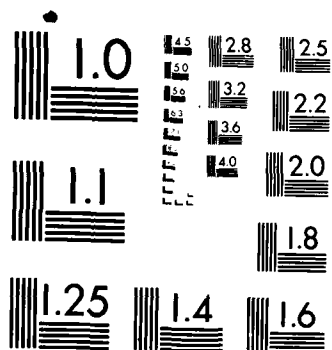FIG. 4.3 RESULTS OF SINGLE-FREQUENCY MEASUREMENT FOR Si AND
GaAs IMPATT DIODES.

END

FILMED

DTIC

MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

power of 9.3 mW at f_1 = 28.69 GHz and I_p = 110 mA. This fundamental frequency is slightly higher than the cutoff frequency of the TE_{20} mode of the waveguide used in the experiment. It was, therefore, possible that, in addition to the TE_{10} mode, the higher mode TE_{20} could also exist within the circuit, but its presence could not be distinguished by the measuring system used. It was found from the measurement that as the fundamental frequency exceeds the cutoff frequency of the TE_{20} mode, the RF output power decreases rapidly. This implies that the presence of higher modes has a significant effect on the measured power level at the fundamental frequency for the Si diodes.

The series resistance of the GaAs diode, according to Adlerstein et al.,[103] could be calculated using the following formula:

$$R_s = \frac{3\alpha'}{\pi\omega^2 C^2 \theta_d} I_s \quad , \tag{4.5}$$

where I_s is the current at the start oscillation condition. For the GaAs diode used, C = 1.03 pF, θ_d = 0.86π, α' = 0.22 V^{-1}, I_s = 130 mA and f_1 = 26.32 GHz. The resulting series resistance was approximately 0.347 Ω. For evaluation of the series resistance of the Si diode used, the value of α' was taken to be equal to the average value for electrons and holes in Si. The values of the other parameters were C = 0.8 pF, θ_d = 0.42 π, I_s = 70 mA and f_1 = 26.32 GHz. The series resistance in that case was 0.44 Ω.

4.4 Measurement of Harmonic Power Generation in Multifrequency

Operation

In order to maximize the RF power at the fundamental or harmonic frequencies, the oscillator circuit should be designed in such a way that it would enable separation of each harmonically related signal and also provide an independent tuning capability at each signal frequency. A simple way of realizing such a circuit is to utilize waveguides as the transmission lines since they possess low loss and specified cutoff frequency properties.

Two different waveguide oscillator circuits were designed for multifrequency operation. One circuit consists of two waveguide sections coupled together and the other circuit consists of three waveguide sections coupled together. Both circuit structures are shown in Fig. 4.4. The waveguide exhibits a high-pass filter property; therefore, it is possible to separate the fundamental and harmonic signals from one another by a proper selection of the waveguide cutoff frequency. The following table shows the cutoff frequency f_c and the useful frequency band f_ω for several waveguides used for oscillator circuit realization.

Table 4.1

Cutoff Frequency and Frequency Band of the Waveguides

Waveguide Type	WR-42	WR-28	WR-22	WR-15	WR-12	WR-10
f_c (GHz)	14.05	21.1	35.35	39.9	48.4	59.05
f_ω (GHz)	18 to 26.5	26.5 to 40	33 to 50	50 to 75	60 to 90	75 to 110
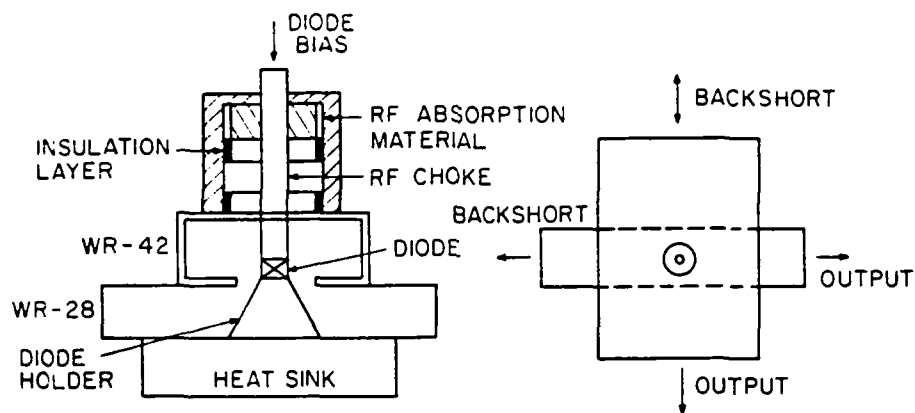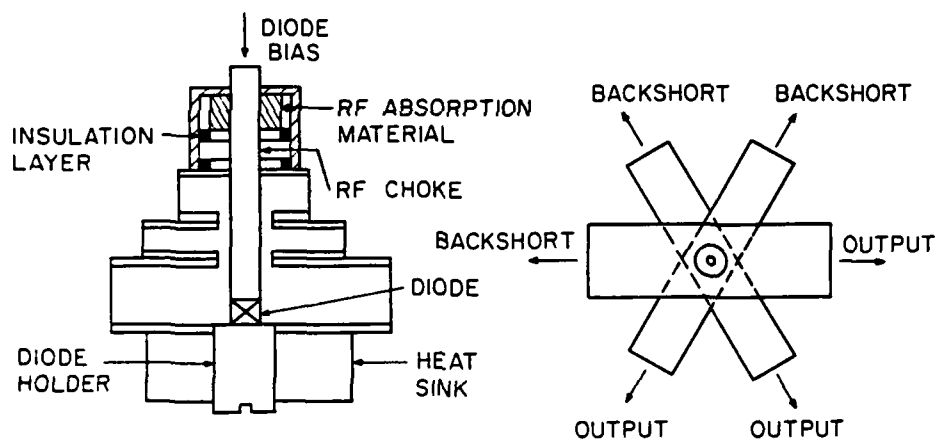
FIG. 4.4 (a) TWO-WAVEGUIDE CIRCUIT FOR MULTIFREQUENCY

MEASUREMENT AND (b) THREE-WAVEGUIDE CIRCUIT FOR

MULTIFREQUENCY MEASUREMENT.

The two-waveguide circuit employs the WR-42 and WR-28-type waveguides. The measurement setup for the two-waveguide circuit is shown in Fig. 4.5. For the fundamental power measurement using the WR-42 waveguide, a metallic short was employed at one port of the E-H tuner connected to the WR-28 waveguide section. For the second harmonic power measurement using the WR-28 waveguide, a metallic short was employed at the E-H tuner, which was connected to the WR-42 waveguide section. Since the operating fundamental frequency of the GaAs diode was approximately 20 GHz, its third-harmonic frequency was approximately 60 GHz. Therefore, it was necessary to insert a section of the WR-12 waveguide into the output of the measuring setup in order to filter out the fundamental and second-harmonic signals from the measured third-harmonic signal.

The GaAs diode was measured under the same pulsed bias current condition as that used for its single-frequency operation. The adjustable backshort and E-H tuner were used at each frequency output in order to ensure the maximum RF power generation. Figure 4.6 shows the measured RF peak power as a function of the pulsed bias current amplitude. The maximum fundamental power obtained from this measurement was 175 mW at $f_1 = 22.587$ GHz with a pulsed bias current of 260 mA. The corresponding efficiency was 2.99 percent. The maximum second-harmonic power obtained was 2 mW at $f_2 = 45.59$ GHz, and the maximum third-harmonic power was 17 μW at $f_3 = 67.69$ GHz. It is noted that the second-harmonic power is 19.4 dB below the fundamental power and the third-harmonic power is 39 dB below the fundamental power. The results obtained are comparable with those predicted by the analytic model discussed in Chapter III.
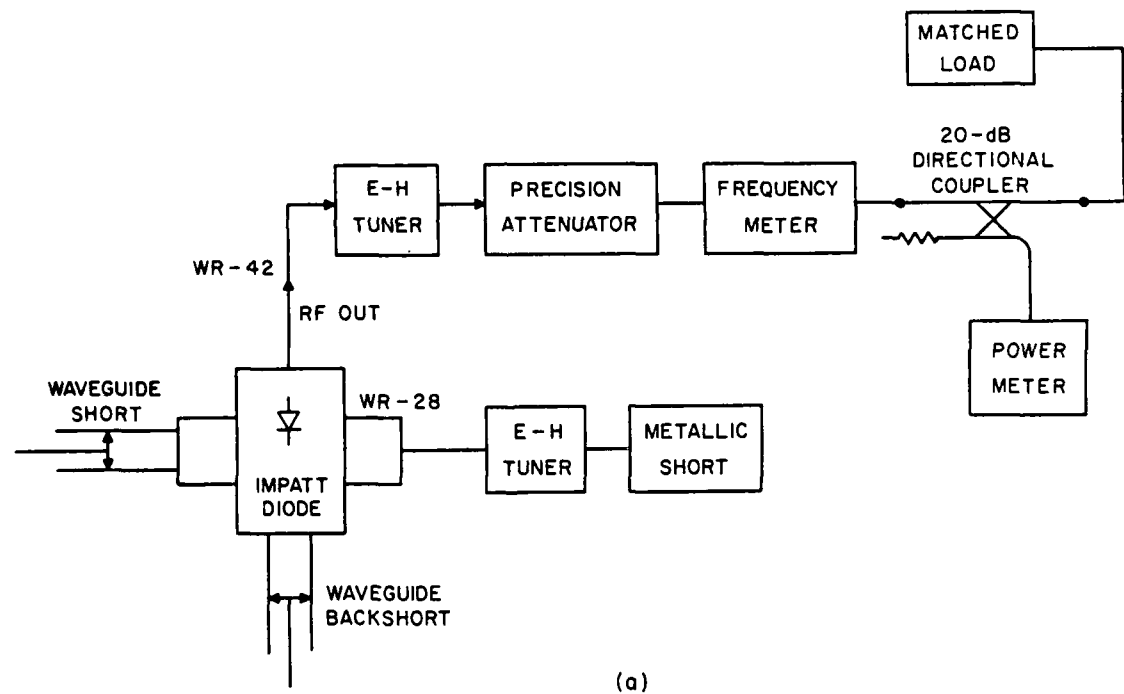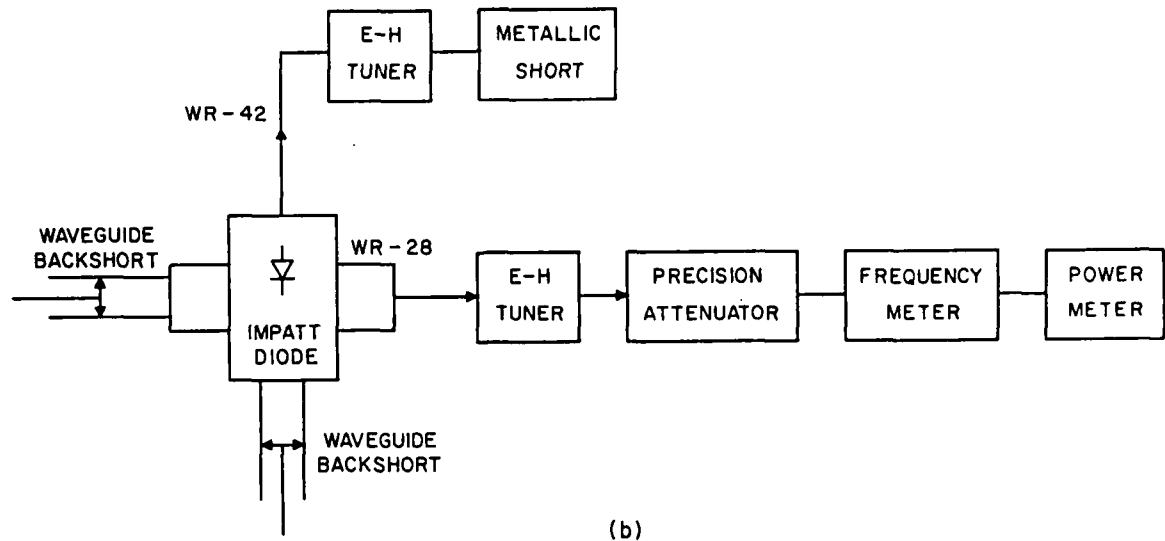
FIG. 4.5 (a) BLOCK DIAGRAM OF THE MEASUREMENT SETUP OF A

TWO-WAVEGUIDE CIRCUIT FOR THE FUNDAMENTAL POWER AND

(b) BLOCK DIAGRAM OF THE MEASUREMENT SETUP OF A TWO-
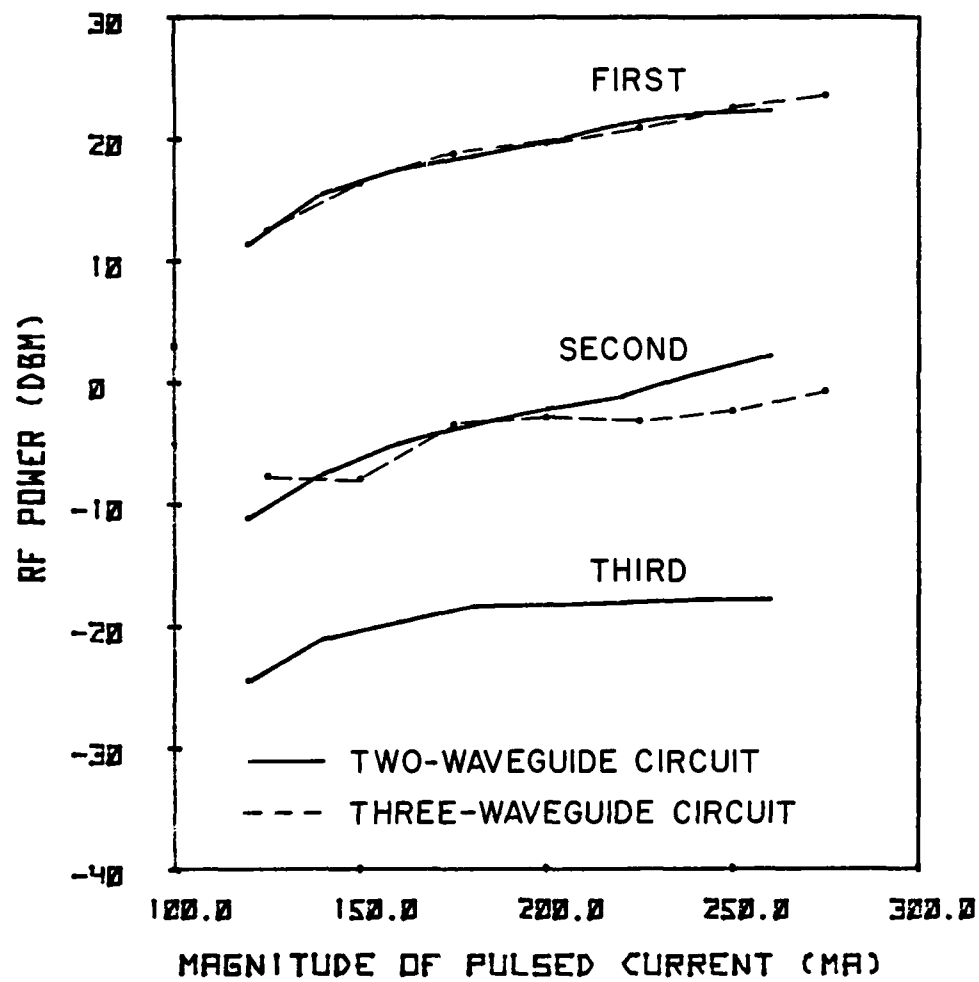
WAVEGUIDE CIRCUIT FOR THE HARMONIC POWER.

FIG. 4.6   MEASURED FUNDAMENTAL AND HARMONIC POWER FROM

THE GaAs IMPATT DIODE.

273-

Qualitatively they are, however, still much lower than those obtained

from the computer simulation discussed in Chapter II.

The operating fundamental frequency of the Si diode was

approximately 30 GHz, which is well above the cutoff frequency of

the TE_{20} mode in the WR-42 waveguide. In this situation, the TE_{20}

mode and subharmonic signal were possibly present in the circuit.

Therefore, an accurate power measurement for the Si diode was difficult

to carry out.

Two three-waveguide oscillator circuits were designed for char-

acterization of the GaAs and Si diodes, respectively. The circuit

used for the GaAs diode consists of WR-42, WR-22 and WR-15 waveguide

sections, and the one used for the Si diode consists of WR-28, WR-15

and WR-12 waveguide sections. The diode heat sink and mounting holder

were placed under the waveguide section (WR-42 or WR-28) employed for

measurement of the fundamental power. The harmonic signals generated

from the diode were coupled to the other waveguide sections via the

mounting post passing through the holes between the waveguides. The

coupling magnitude between the waveguides depended on the post and

hole diameters. A large post diameter introduced a small inductance

to the circuit. The hole diameter in the three-waveguide circuit

discussed was restricted by the actual width of the narrowest wave-

guide used in the circuit. The ratio between the post and the hole

diameters was kept around 0.7. By reducing this ratio, the increase

of the capacitance between the post and the holes leads in consequence

to the increase of the coupling magnitude between waveguide sections

for the fundamental and harmonic signals. By increasing this ratio,

the power at the fundamental is decreased.

The measurement setup for the GaAs diode is shown in Fig. 4.7. The diode was biased in the same manner as for the two-waveguide circuit. The RF power at each frequency was measured using reactive terminations at the remaining signal ports. The measured RF peak power values obtained are shown in Fig. 4.6. The maximum fundamental power was 235 mW at f_1 = 26.14 GHz with a current of 275 mA. The corresponding second-harmonic power was 0.87 mW at f_2 = 50.95 GHz, but the third-harmonic power was too small to be detected.

The second-harmonic power measured for the GaAs diode in the three-waveguide circuit is smaller than that obtained from the two-waveguide circuit. The difference is probably due to the coupling magnitude between the waveguide sections designated for the fundamental and second-harmonic signals. In the three-waveguide circuit, the waveguide sections for the fundamental and second-harmonic signals were separated from each other by that for the third-harmonic signal. This, in turn, caused an increase of the circuit reactance presented to the diode at the second harmonic and reduced the coupling between the waveguide sections for the fundamental and second-harmonic signals. The reason for a low level of the third-harmonic power below the detection level was probably due to the fact that the fundamental waveguide section was too long so that the third-harmonic power was dissipated in this waveguide section rather than being coupled to the third-harmonic waveguide (WR-15).

For the Si diode, the measurement of the fundamental and harmonic powers was conducted using the following procedures:

1. Simultaneous measurements were performed of the RF power at the fundamental and harmonic frequency without using a reactive
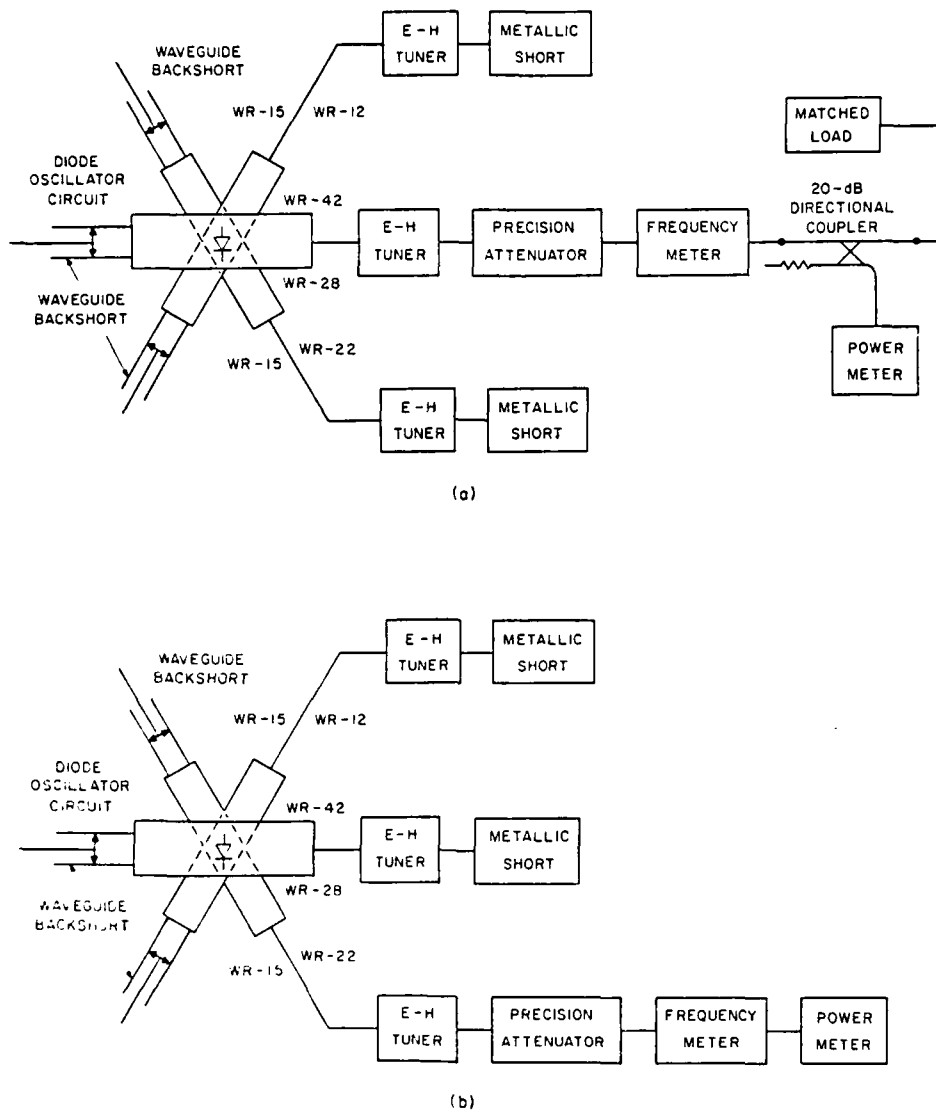
FIG. 4.7 (a) BLOCK DIAGRAM OF MEASUREMENT SETUP OF THREE-
WAVEGUIDE CIRCUIT FOR FUNDAMENTAL POWER AND (b)
BLOCK DIAGRAM OF MEASUREMENT SETUP OF THREE-
WAVEGUIDE CIRCUIT FOR HARMONIC POWER.

termination for any signal. The corresponding measurement setup is shown in Fig. 4.8.

2. The RF power was measured at each frequency employing reactive terminations for the remaining two signals. The corresponding measurement setup is similar to that shown in Fig. 4.7.

The measured results are shown in Fig. 4.9. The best result obtained for the power at the fundamental frequency was 15 mW at $f_1 = 32.43$ GHz. The maximum level for the second-harmonic signal power was 0.17 mW at $f_2 = 64.95$ GHz. The maximum power at the third harmonic was 2.2 μW.

4.5 Discussion

The results obtained indicate that the GaAs and Si diodes did not generate a significant amount of the RF power at the fundamental and harmonic frequencies, which could mean that the diodes did not operate at their optimum conditions. The possible reasons for that situation are discussed in the following:

1. The effect of diode series resistance. From the calculation made previously, the series resistance of the GaAs diodes is approximately equal to 0.347 Ω, which is relatively large for this device. The series resistance of the Si diode, which has a nonpunch-through structure, is approximately equal to 0.44 Ω. A large value of the series resistance restricts the RF voltage swing in the diode so that the depletion-layer modulation effect cannot take place and also absorbs much of the useful RF power. Consequently, the harmonic current generation is limited and the harmonic power delivered to the output is small. By increasing the dc current it is possible to increase
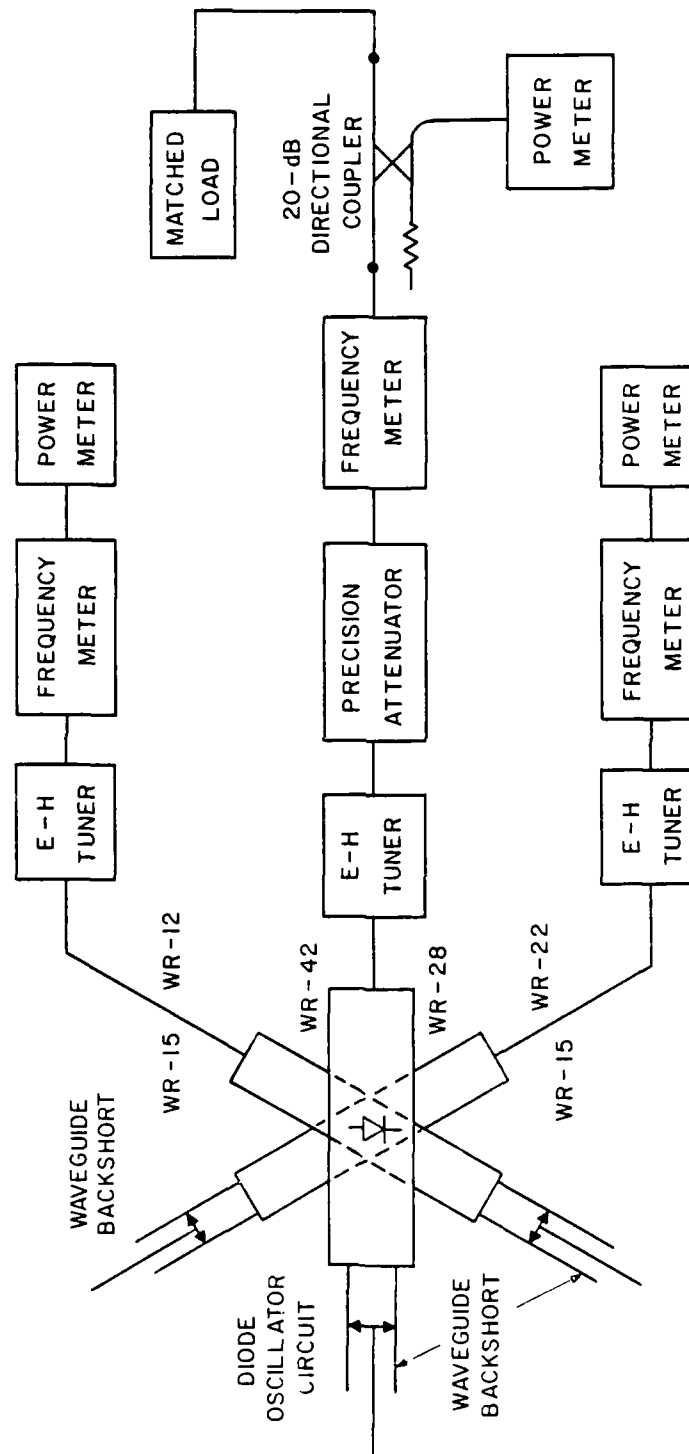
FIG. 4.8 BLOCK DIAGRAM OF MEASUREMENT SETUP OF THREE-WAVEGUIDE CIRCUIT FOR Si IMPATT DIODES.
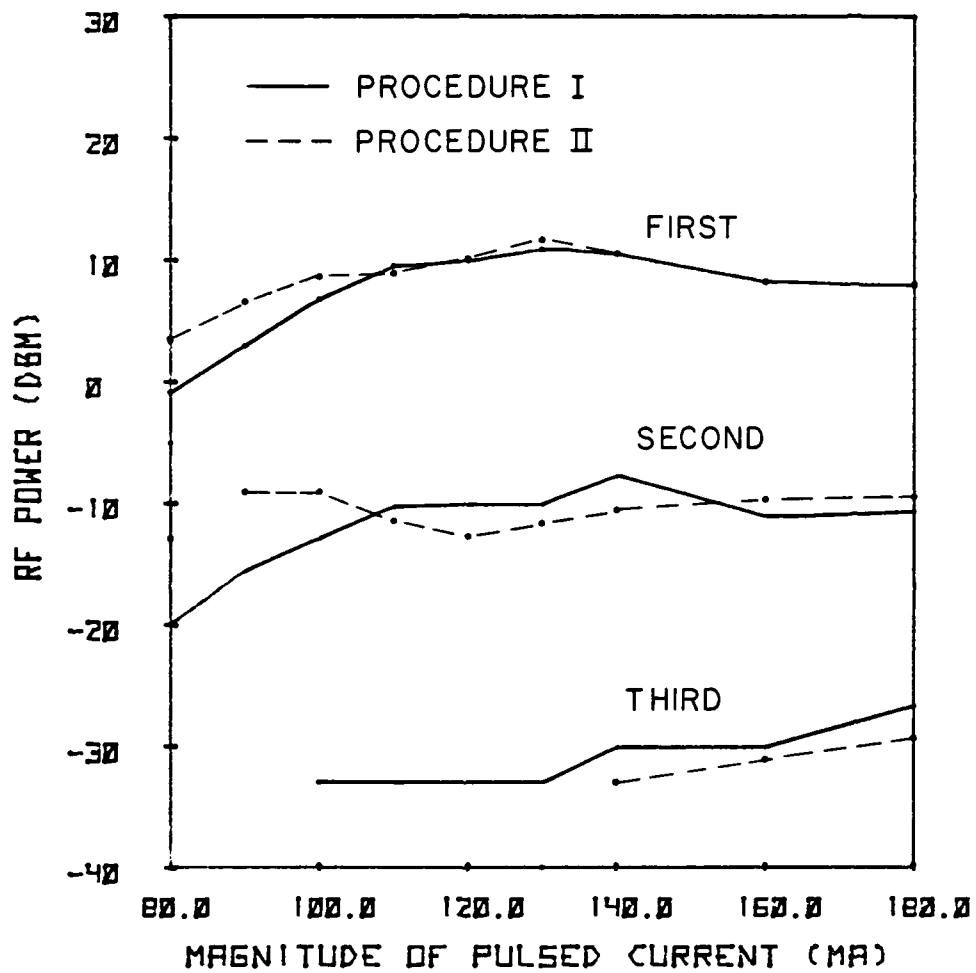
FIG. 4.9 MEASURED FUNDAMENTAL AND HARMONIC POWERS FROM

THE Si DIODE.

the harmonic power, but it can lead to an excessive temperature in the diodes. Furthermore, the effect of low-frequency instability also prevents a high pulsed current from being used. It can be concluded that the best way to improve the RF power level at harmonic frequencies is to reduce the diode series resistance.

2. Matching and coupling structure. In order to measure the RF power at the harmonic frequencies, the oscillator circuit should not only provide a proper impedance level to match the diode at the optimum condition, but it should also assure proper coupling between the waveguide sections at the fundamental and harmonic frequencies. The coupling in the circuit was via the metallic post and the holes between the waveguide sections. The coupling hole for the fundamental frequency waveguide section contributes a significant discontinuity capacitance, which in turn affects the diode performance at the fundamental frequency. Therefore, a tradeoff must be made between the diameters of the post and holes in order to arrive at an optimum condition for maximum RF harmonic power. In addition, by placing the harmonic frequency waveguide section as close as possible to the fundamental frequency waveguide section, the effect of reduced post inductance leads to an increase of harmonic power. Keeping the fundamental frequency waveguide section as short as possible can also improve the RF power loss, particularly at the harmonic frequencies.

3. Diode biasing circuit. Low-frequency oscillation creates a serious problem especially when using the GaAs diodes. It was observed that, for the GaAs diode, when the pulsed current exceeded a certain level (approximately 180 mA), the low-frequency oscillation

occurred in the circuit. With the presence of this type of instability, the RF power level drops dramatically due to the parametric effects between the low-frequency and fundamental-frequency signals. Consequently, this effect imposes a limit on the maximum current that can be applied to the diode without causing any serious damage to the diode. The best way to suppress the low-frequency instability is to increase the bias circuit resistance for frequencies in the MHz region by using RF absorption material in the circuit and properly designing the bias choke.

CHAPTER V

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

5.1 Conclusions

The objective of this study was to investigate the harmonic power generation capability of IMPATT diodes of various structures. Both theoretical calculations and experimental investigations were conducted to accomplish this goal. In this chapter, the most significant conclusions are reviewed and some suggestions for future work are discussed.

The first part of Chapter II was devoted to the problem of conventional IMPATT diodes having different doping structures. The effects of avalanche multiplication, the drift process, and depletion-layer modulation were discussed in terms of the diode single-frequency operation. The first two mechanisms are important for performance at the fundamental frequency, but the latter one is essential for harmonic signal generation. In order to induce a depletion-layer modulation effect, the diode should be driven at a high level of fundamental frequency voltage. The depletion-layer modulation effect also can be affected by the presence of a harmonic voltage signal. In order to maintain the diode in the active mode of operation, the applied harmonic voltage must properly delay the onset of the depletion-layer modulation. For third-harmonic performance, this will increase the phase delay of the third-harmonic current and decrease the amplitude of the third-harmonic current. The third-harmonic power generation tends to saturate at a certain level of

the third-harmonic voltage. Because of a small dependence of the third-harmonic current on the third-harmonic voltage level, the GaAs and Si uniform diodes exhibit better third-harmonic performance than the GaAs double-Read and Si hybrid diodes. The GaAs uniform diode attains the highest third-harmonic efficiency because of the field-dependent velocity characteristic of the electrons of the GaAs material. The Si uniform diode gives the highest third-harmonic power because of the high thermal conductivity and saturated velocity levels of the Si material.

The second part of Chapter II was devoted to the investigation of the pin diode structure operated in a passive mode. The diode performance for different device lengths in single-frequency operation was calculated and compared in terms of space-charge and transit-time effects. The device length determines the device RF power performance, since it determines the space-charge and transit-time effects, both of which in turn affect the build-up and fall-off of the induced current. For a long length diode structure, both effects significantly degrade the harmonic current generation. The harmonic current generation can be improved by reducing the device length, but the corresponding device impedance level will decrease proportionally. An appropriate third-harmonic voltage can also improve the third-harmonic current generation by improving the induced current waveform. These improvements are limited by the fact that the third-harmonic current amplitude cannot exceed twice the dc current. Therefore, the diode will achieve the optimum third-harmonic power generation for a certain device length. This optimum device length depends

LIST OF REFERENCES

1.   Shockley, W., "Negative Resistance Arising from Transit Time
      in Semiconductor Diodes," Bell System Tech. J., vol. 33, No. 4,
      pp. 799-826, July 1954.

2.   Coleman, D. J., Jr. and Sze, S. M., "A Low-Noise Metal-
      Semiconductor-Metal (MSM) Microwave Oscillator," Bell System
      Tech. J. (Brief), vol. 50, No. 5, pp. 1695-1699, May-June 1971.

3.   Read, W. J., "A Proposed High Frequency Negative Resistance Diode,"
      Bell System Tech. J., vol. 37, No. 2, pp. 401-446, March 1958.

4.   Johnston, R. L., DeLoach, B. C., Jr. and Cohen, B. G., "A
      Silicon Diode Microwave Oscillator," Bell System Tech. J.,
      vol. 44, No. 2, pp. 369-372, February 1965.

5.   Swan, C. B., "Improved Performance of Silicon Avalanche
      Oscillators Mounted on Diamond Heat Sink," Proc. IEEE
      (Correspondence), vol. 55, No. 9, pp. 1617-1618, September 1967.

6.   Dilorenzo, J. V., Niehaus, W. C., Velebir, J. R. and Iglesias,
      D. E., "Beam Lead Plated Heat Sink GaAs IMPATT: Part I--Perfor-
      mance," IEEE Trans. on Electron Devices, vol. ED-22, No. 8,
      pp. 509-514, August 1975.

7.   Panish, M. G. and Cho, A. Y., "Molecular Beam Epitaxy," IEEE
      Spectrum, vol. 17, No. 4, pp. 18-23, April 1980.

8.   Evans, W. J., "Nonlinear and Frequency Conversion Characteris-
      tics of IMPATT Diodes," Tech. Report No. 104, Electron Physics
      Laboratory, The University of Michigan, Ann Arbor, 1968.

9.   Fisher, S. T., "Small-Signal Impedance of Avalanching Junctions
      with Unequal Electron and Hole Ionization Rates," IEEE Trans. on
      Electron Devices, vol. ED-14, No. 6, pp. 313-322, June 1967.

10.   Gummel, H. K. and Blue, J. L., "A Small-Signal Theory of Avalanche
      Noise in IMPATT Diodes," IEEE Trans. on Electron Devices, vol.
      ED-14, No. 9, pp. 569-580, September 1967.

11.   Shroeder, W. E. and Haddad, G. I., "Nonlinear Properties of
      IMPATT Diodes" (Invited Paper), Proc. IEEE, vol. 61, No. 2,
      pp. 153-182, February 1973.

12.   Scharfetter, D. L. and Gummel, H. K., "Large-Signal Analysis of
      a Silicon Read Diode Oscillator," IEEE Trans. on Electron Devices,
      vol. ED-16, No. 1, pp. 64-77, January 1969.

13. Schroeder, W. E., "Nonlinear Properties of IMPATT Diodes," Tech. Report No. 126, Electron Physics Laboratory, The University of Michigan, Ann Arbor, 1972.

14. Mains, R. K., Haddad, G. I. and Blakey, P. A., "Simulation of GaAs IMPATT Diodes Including Energy and Velocity Transport Equations," IEEE Trans. on Electron Devices, vol. ED-30, No. 10, pp. 1327-1338, October 1983.

15. Sze, S. M., Physics of Semiconductor Devices, 2nd Ed., John Wiley and Sons, Inc., New York, 1981.

16. Adlerstein, M. G., McClymonds, J. W. and Massé, D., "Gallium Arsenide IMPATT Diodes at 20 GHz," IEEE/MTT-S Int. Microwave Symposium Digest, Dallas, TX, pp. 143-145, June 1982.

17. Adlerstein, M. G. and Moore, E. L., "Microwave Properties of GaAs IMPATT Diodes at 33 GHz," Proc. 8th Biennial Cornell Elec. Eng. Conf. on Microwave Semiconductor Devices and Circuits, Ithaca, NY, pp. 375-384, August 1981.

18. Adlerstein, M. G. and Chu, S.L.G., "GaAs IMPATT Diodes for 60 GHz," IEEE Electron Device Letters, vol. EDL-5, No. 3, pp. 97-98, March 1984.

19. Swan, C. B., "IMPATT Oscillator Performance Improvement with Second Harmonic Tuning," Proc. IEEE (Correspondence), vol. 56, No. 9, pp. 1616-1617, September 1968.

20. Blue, J. L., "Approximate Large-Signal Analysis of IMPATT Oscillators," Bell System Tech. J., vol. 48, No. 2, pp. 383-396, February 1969.

21. Schroeder, W. E. and Haddad, G. I., "Effects of Harmonic and Subharmonic Signals on Avalanche-Diode Oscillator Performance," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-18, No. 6, pp. 327-331, June 1970.

22. Kuvås, R. and Lee, C. A., "Nonlinear Analysis of Multifrequency Operation of Read Diodes," J. Appl. Phys., vol. 41, No. 4, pp. 1756-1767, 15 March 1970.

23. Mouthaan, K., "Characterization of Nonlinear Interactions in Avalanche Transit Time Oscillators, Frequency Multipliers and Frequency Dividers," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-18, No. 11, pp. 853-862, November 1970.

24. Mouthaan, K., "Nonlinear Characteristics and Two-Frequency Operation of the Avalanche Transit-Time Oscillators," Phillips Research Reports, vol. 25, pp. 33-67, February 1970.

on the operating fundamental frequency, but seems to be less dependent
on the dc current density at low dc current density levels.

In Chapter III, an analytic model for three-frequency operation
was developed to investigate the small- and large-signal performances
of a GaAs double-Read diode under the presence of harmonic signals.
For achieving better third-harmonic power generation, a large amplitude
of fundamental frequency voltage is required. However, because of the
lack of the depletion-layer modulation effect, the third-harmonic
output power obtained is low. The presence of a proper second-harmonic
voltage can improve the third-harmonic output power to some extent,
but the presence of diode series resistance significantly reduces the
available RF output power. Since the harmonic voltages are usually
small in magnitude compared to the operating fundamental voltage,
the stability of the oscillator was found to be strongly dependent on
the fundamental frequency operating circuit conditions.

In Chapter IV, several waveguide circuits were designed for
measurement of the RF output power of the GaAs double-Read diodes and
Si single-drift uniform diodes. These diodes were found to have
high series resistances. Hence the measured harmonic power was low.
It was found that the coupling structure of the circuit should be
optimized in order to obtain better power performance.

5.2 Suggestions for Future Work

In order to optimize the power generation at the harmonic
frequencies using IMPATT diodes, the following future research is
recommended. For conventional IMPATT diodes, the Si diode with
uniformly doped structure appears to be the most promising diode

for harmonic power generation. It is believed that optimizing the punch-through factors on both the p and n sides of the diode can further improve the harmonic power generation. Pulsed mode operation is another area worthy of investigation in order to gain further understanding of the limitations of the conventional IMPATT and pin diode structures for harmonic power generation. Definitely, in pulsed mode operation, the space-charge effect has a great influence on the diode performance. It is noted that, in the millimeter-wave frequency range, the drift-diffusion model employed for computer simulation is still valid for the Si diodes, but some corrections are needed for the GaAs diodes. If the depletion-layer modulation effect could be modeled properly, the analytic model proposed would also be useful for analyzing the diode performance under the high RF voltage swing conditions. It would be interesting to obtain practically some uniformly doped IMPATT diodes and pin diodes with different lengths. The immediate need for this is to develop a technique that would reduce significantly the series resistance inherent in the diodes and to design a waveguide circuit with improved coupling between waveguide sections without degradation of the diode performance, assuring an independent circuit adjustment at each signal frequency.

25. Brackett, C. A., "Characterization of Second Harmonic Effects in IMPATT Diodes," Bell System Tech. J., vol. 58, No. 10, pp. 1777-1810, October 1970.

26. Kurokawa, K. and Magalhaes, F. M., "An X-Band 10-Watt Multiple-IMPATT Oscillator," Proc. IEEE (Letter), vol. 59, No. 1, pp. 102-107, January 1971.

27. Peterson, D. F., "Harmonic Power Combining of Microwave Solid State Active Devices," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-30, No. 3, pp. 260-268, March 1982.

28. Seidel, T. E., Niehaus, W. C. and Iglesias, D. E., "Double-Drift Silicon IMPATT's at X-Band," IEEE Trans. on Electron Devices, vol. ED-21, No. 8, pp. 523-531, August 1974.

29. Ying, R. S., "X-Band Silicon Double-Drift IMPATT Diodes Using Multiple Epitaxy," Proc. IEEE (Correspondence), vol. 60, No. 9, pp. 1104-1105, September 1972.

30. Pfund, G., Snapp, C. and Podell, A., "Pulsed and CW Double-Drift Silicon IMPATTs," IEEE S-MTT Int. Microwave Symp., Atlanta, GA, pp. 312-313, June 1974.

31. Seidel, T. E. and Niehaus, W. C., "Double-Drift Silicon Diodes at X-Band," Presented at the Device Research Conf., Boulder, CO, June 1973.

32. Midford, T. A. and Bernick, R. L., "Millimeter-Wave CW IMPATT Diodes and Oscillators," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-27, No. 5, pp. 483-492, May 1979.

33. Seidel, T. E., Davis, R. E. and Iglesias, D. E., "Double-Drift-Region Ion-Implanted Millimeter-Wave IMPATT Diodes," Proc. IEEE, vol. 59, No. 8, pp. 1222-1228, August 1971.

34. Hirachi, Y., Tōyama, Y., Fukukawa, Y. and Tokumitsu, Y., "A High Power 50 GHz DDR IMPATT Oscillator with Low Side Band Noise," IEEE-MTT-S Int. Microwave Symp., Cherry Hill, NJ, pp. 36-39, June 1976.

35. Leistner, D., "Efficient P-Type Si IMPATT Diodes for V-Band Frequencies," Electronics Letters, vol. 17, No. 18, pp. 635-636, 3 September 1981.

36. Howard, A. M., Smith, D. J. and Purcell, J. J., "Epitaxially Grown Double-Drift Silicon IMPATT Diodes at 60 to 90 GHz," Electronics Letters, vol. 10, No. 21, pp. 443-445, 17 October 1974.

37. Ino, M., Makimura, T., Ishibashi, T. and Ohmori, M., "80 GHz Silicon Diamond Heatsink IMPATT Diodes," Electronics Letters, vol. 15, No. 1, pp. 2-3, 4 January 1979.

38. Gokgor, H. S., Davies, I., Howard, A. M. and Brookbanks, D. M., "High-Efficiency Millimeter-Wave Silicon IMPATT Diode Oscillators," Electronics Letters, vol. 17, No. 20, pp. 744-745, 1 October 1981.

39. Chang, K., Thrower, W. F. and Hayashibara, G. M., "Millimeter-Wave Silicon IMPATT Sources and Combiners for 110-200 GHz Range," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-29, No. 12, pp. 1278-1284, December 1981.

40. Ino, M., Ishibashi, T. and Ohmori, M., "CW Oscillator with p^+-n-p^+ Silicon IMPATT Diodes in 200 GHz and 300 GHz Bands," Electronics Letters, vol. 12, No. 6, pp. 148-149, 18 March 1976.

41. Ishibashi, T. and Ohmori, M., "200-GHz 50-mW CW Oscillator with Silicon SDR IMPATT Diodes," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-24, No. 11, pp. 858-859, November 1976.

42. Ishibashi, T., Ino, M., Makimura, T. and Ohmori, M., "Liquid-Nitrogen-Cooled Submillimeter-Wave Silicon IMPATT Diodes," Electronics Letters, vol. 10, pp. 299-300, 12 May 1977.

43. Gilden, M. and Moroney, W., "High Power Pulsed Avalanche Diode Oscillators for Microwave Frequencies," Proc. IEEE (Letters), vol. 55, No. 6, pp. 1227-1228, July 1967.

44. Pfund, G. and Curby, R., "High Peak Pulse Power Silicon Double-Drift IMPATT Diodes," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-29, No. 5, pp. 450-452, May 1979.

45. Nagao, H., Hasumi, H. and Fujine, N., "X-Band 50 W Silicon Double Drift Pulsed Region IMPATT Diode," Int. Solid-State Circuits Conf. Digest of Tech. Papers, Philadelphia, PA, pp. 168-169, February 1979.

46. Pfund, G., Snapp, C. D. and Podell, A., "Pulsed Double-Drift Silicon IMPATT Diodes and Their Applications," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-22, No. 12, pp. 1134-1140, December 1974.

47. Walker, J.L.B. and Hing, A., "A 31 W Peak 35 GHz Silicon Double-Drift IMPATT Diode," Proc. 8th Biennial Cornell Electrical Engineering Conf. on Microwave Semiconductor Devices and Circuits, Ithaca, NY, pp. 371-373, August 1981.

48. Freyer, J., Kasper, E. and Barth, H., "Pulsed V-Band MBE Si IMPATT Diodes," _Electronics Letters_, vol. 16, No. 22, pp. 865-866, 6 November 1980.

49. Chang, K., Sun, C., English, D. L. and Nakaji, L. M., "High Power 94-GHz Pulsed IMPATT Oscillators," _IEEE MTT-S Int. Microwave Symp._, Orlando, FL, pp. 71-72, April-May 1979.

50. Adlerstein, M. G., Wallace, R. N. and Steele, S. R., "High-Power C Band Read IMPATT Diodes," _Electronics Letters_, vol. 11, No. 18, pp. 430-431, 4 September 1975.

51. Nishitani, K., Sawano, H., Ishii, T. and Mitsui, S., "Highly Reliable 10 W and 30% p-n Junction GaAs Read Diode," Presented at the Device Research Conf., Ithaca, NY, June 1976.

52. Hirachi, Y., Kobayashi, K., Ogasawara, K., Hisatsugu, T. and Toyama, Y., "A New Operation Mode: Surfing Mode in High-Low Type GaAs IMPATTs, _IEEE Int. Electron Devices Meeting Tech. Digest_, Washington, DC, pp. 102-105, December 1976.

53. Wallace, R. N., Steele, S. R. and Adlerstein, M. C., "Performance of GaAs Double-Drift Avalanche Diodes," _Proc. Sixth Biennial Cornell Electrical Engineering Conf. on Active Microwave Semiconductor Devices and Circuits_, Ithaca, NY, pp. 195-199, August 1977.

54. Kim, C. K. and Matthei, W. G., "GaAs Read IMPATT Diode Oscillators," _Proc. Fourth Biennial Electrical Engineering Conf._, Ithaca, NY, pp. 299-305, August 1973.

55. Grierson, J. R., Cooper, K., Leigh, P. A., O'Sullivan, P. J. and Huish, P. N., "High Power 11 GHz GaAs Hi-Lo IMPATT Diodes with Titanium Schottky Barriers," _Electronics Letters_, vol. 15, No. 1, pp. 13-14, January 1979.

56. Kim, C., Steele, R. and Bierig, R., "High Power High Efficiency Operation of Read-Type IMPATT-Diode Oscillators," _Electronics Letters_, vol. 95, No. 8, pp. 173-174, 3 May 1973.

57. Berenz, J. J., Vichr, M. and Fank, F. B., "Comparison of GaAs IMPATT Designs for 20 GHz," _Electronics Letters_, vol. 15, No. 21, pp. 694-695, 11 October 1979.

58. Ma, Y. E., Benko, E. and Trinh, T., "High Efficiency V-Band GaAs IMPATT Diodes," _Electronics Letters_, vol. 20, No. 5, pp. 212-214, 1 March 1984.

59. Zhang, X. and Freyer, J., "0.7 W Single-Drift GaAs IMPATT Diodes for Millimeter-Wave Frequencies," _Electronics Letters_, vol. 20, No. 9, pp. 369-360, 26 April 1984.

60. Elta, M. E., Fetterman, H. R., Macropoulos, ¨. V. and Lambert, J. J., "150 GHz GaAs MITATT Source," IEEE Electron Device Letters, vol. EDL-1, No. 6, pp. 115-116, June 1980.

61. Berenz, J. J., Kinoshita, J., Hierl, T. L. and Frank, F. B., "High-Power Pulsed GaAs Double-Drift Hybrid-Read IMPATT Diodes for X-Band," Electronics Letters, vol. 15, No. 10, pp. 277-278, 10 May 1979.

62. Hierl, T. L., Berenz, J. J. and Long, S. I., "GaAs Pulsed Read IMPATT Diodes," Proc. Sixth Biennial Cornell Electrical Engineering Conf. on Active Microwave Semiconductor Devices and Circuits, Ithaca, NY, pp. 211-219, August 1977.

63. Schawarz, R. I. and Bonek, E., "Current-Tuned GaAs Schottky-Barrier IMPATT Diodes for 60-90 GHz Operation." Electronics Letters, vol. 14, No. 25, pp. 812-813, 7 December 1978.

64. Nishizawa, J. I., Motoya, K. and Okuno, Y., "GaAs TUNNETT Diodes," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-26, No. 12, pp. 1029-1035, December 1977.

65. Moncrief, F. J., "Technology Review Semiconductors," Microwaves, vol. 18, No. 8, pp. 21, August 1979.

66. Bauhahn, P. E., "Properties of Semiconductor Materials and Transit Time Devices," Tech. Report No. 140, Electron Physics Laboratory, The University of Michigan, Ann Arbor, October 1977.

67. Mains, R. K. and Haddad, G. I., "Properties of High Efficiency X-Band GaAs IMPATT Diodes," Tech. Report No. AFAL-TR-81-1066, Electron Physics Laboratory, The University of Michigan, Ann Arbor, June 1981.

68. Mains, R. K., Private communication.

69. Lee, C. A., Logan, R. A., Batdorf, R. L., Kleimack, J. J. and Wiegmann, W., "Ionization Rates of Holes and Electrons in Silicon," Phys. Rev., vol. 134, pp. A761-A773, May 4, 1964.

70. van Overstraeten, R. and DeMan, H. J., "Measurement of Ionization Rates in Diffused Silicon, p-n Junction," Solid-State Electronics, vol. 13, No. 5, pp. 583-608, May 1970.

71. Grant, W. N., "Electron and Hole Ionization Rates in Epitaxial Silicon at High Electric Fields," Solid-State Electronics, vol. 16, No. 10, pp. 1189-1203, October 1973.

72. Seddik, M. M. and Haddad, G. I., "Effects of Ionization Rates on IMPATT Device Admittance," IEEE Trans. on Electron Devices, vol. ED-20, No. 12, pp. 1164-1168, December 1973.

73. Mains, R. K. and Haddad, G. I., "Capabilities and Potential of Millimeter-Wave IMPATT Devices," Tech. Report No. AFAL-TR-82-1141, Electron Physics Laboratory, The University of Michigan, Ann Arbor, August 1982.

74. Baraff, G. A., "Distribution Junction and Ionization Rates for Holes and Electrons in Semiconductors," Phys. Rev., vol. 128, No. 6, pp. 2507-2517, June 1962.

75. Kuvås, R. L. and Schroeder, W. E., "Premature Collection Mode in IMPATT Diodes," IEEE Trans. on Electron Devices, vol. ED-22, No. 8, pp. 549-558, August 1975.

76. Schroeder, W. E. and Haddad, G. I., "Nonlinear Properties of IMPATT Devices" (Invited Paper), Proc. IEEE, vol. 61, No. 2, pp. 153-169, February 1973.

77. Culshaw, B., Giblin, R. A. and Blakey, P. A., Avalanche Diode Oscillators, Taylor and Francis Ltd., London, 1978.

78. Kreyszig, E., Advanced Engineering Mathematics, Third Edition, John Wiley and Sons, Inc., New York, 1972.

79. Misawa, T., "High Frequency Fall-Off of IMPATT Diode Efficiency," Solid-State Electronics, vol. 15, No. 4, pp. 457-465, April 1972.

80. Statz, H., Haus, H. and Pucell, R., "Large-Signal Dynamic Loss in Gallium Arsenide Read Avalanche Diodes," IEEE Trans. on Electron Devices, vol. ED-25, No. 1, pp. 23-33, January 1978.

81. Zhang, X. and Freyer, J., "0.7 W Single-Drift GaAs IMPATT Diode for Millimeter-Wave Frequencies," Electronics Letters, vol. 20, No. 9, pp. 369-360, April 1984.

82. Kennedy, D. P., "Spreading Resistance in Cylindrical Semiconductor Devices," J. Appl. Phys., vol. 31, No. 8, pp. 1490-1497, August 1960.

83. Olson, H. M., "Temperature Transients in IMPATT Diodes," IEEE Trans. on Electron Devices, vol. ED-23, No. 5, pp. 485-503, May 1976.

84. Maycock, P. P., "Thermal Conductivity of Silicon Germanium III-V Compounds and III-V Alloys," Solid-State Electronics, vol. 10, No. 3, pp. 161-168, March 1967.

85. Ntake, P. L. and Cohn, D. R., "Frequency Multiplication by a pin Diode when Driven into Avalanche Breakdown," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-13, No. 6, pp. 477-485, June 1975.

86. Burckhardt, C. B., "Analysis of Varactor Frequency Multipliers for Arbitrary Capacitance Variation and Drive Level," _Bell Sys. Tech. J._, vol. 44, pp. 675-692, April 1966.

87. Scanlan, J. O., "Analysis of Varactor Harmonic Generation," _Advances in Microwaves_, vol. 2, pp. 115-236, Academic Press, Inc., New York, 1967.

88. Misawa, T., "Negative Resistance in p-n Junction under Avalanche Breakdown Conditions, Parts I and II," _IEEE Trans. on Electron Devices_, vol. ED-13, No. 1, pp. 169-175, January 1966.

89. Penfield, P., Jr. and Rafuse, R. P., _Varactor Applications_, The MIT Press, Cambridge, 1962.

90. Schroeder, W., "Nonlinear Properties of IMPATT Devices," Ph.D. Dissertation, Electron Physics Laboratory, The University of Michigan, Ann Arbor, 1972.

91. Gilden, M. and Hines, M. E., "Electronic Tuning Effects in the Read Microwave Avalanche Diode," _IEEE Trans. on Electron Devices_, vol. ED-13, No. 1, pp. 169-175, January 1966.

92. Kurokawa, K., "Some Basic Characteristics of Broadband Negative Resistance Oscillator Circuits," _Bell System Tech. J._, vol. 48, No. 7, pp. 1937-1965, July 1969.

93. Bates. B. P. and Khan, P. J., "Stability of Multifrequency Negative-Resistance Oscillators," _IEEE Trans. on Microwave Theory and Techniques_, vol. MTT-32, No. 10, pp. 1310-1319, October 1984.

94. Allen, P. J., Bates, B. D. and Khan, P. J., "Analysis and Use of Harkless Diode Mount for IMPATT Oscillators," _IEEE MTT-S Int. Microwave Digest_, Dallas, TX, pp. 138-141, June 1982.

95. Ohmori, M., Niizuma, H., Ishii, Y. and Suzuki, K., "New Functional Operations with Avalanche Diodes," _Proc. Second Conf. on Solid State Devices_, Tokyo, Japan, pp. 221-226, 1970.

96. Bowman, L. S. and Muller, H. J., "Oscillator of Silicon pn Junction Avalanche Diodes in 50 to 140 GHz Range," _Proc. IEEE_, vol. 54, No. 8, pp. 1080-1081, August 1966.

97. Birch, J. R., "Free Space Video Detection of Harmonic Content of 100 GHz IMPATT Oscillator," _Electronics Letters_, vol. 16, No. 21, pp. 799-800, 9 October 1980.

98. Blakey, P. A., East, J. R., Haddad, G. I., Heaton, J. and Kinzel, D., "Computerized C(V) Profiling Techniques," _Proc. Seventh Biennial Conf. on Active Microwave Semiconductor Devices and Circuits_, Ithaca, NY, pp. 238-245, August 1979.

99. Lewin, L., "A Contribution to the Theory of Probes in Waveguides," Proc. IEE, vol. 104, No. 10, pp. 109-116, October 1957.

100. Eisenhart, R. J. and Khan, P., "Theoretical and Experimental Analysis of a Waveguide Mounting Structure," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-19, No. 8, pp. 706-718, August 1974.

101. Williamson, A. G., "Analysis and Modeling of a Single-Post Wave-guide Mounting Structure," Proc. IEE, vol. 129, No. 5, pp. 271-277, October 1982.

102. Collin, R. E., Foundations for Microwave Engineering, McGraw-Hill Book Co., Inc., New York, 1960.

103. Adlerstein, M. G., Holwag, L. H. and Chu, S.L.G., "Measurement of Series Resistance in IMPATT Diodes," IEEE Trans. on Electron Devices, vol. ED-30, No. 2, pp. 179-182, February 1983.

Publications

"Optimum Design of Millimeter-Wave IMPATT Diode Oscillators,"
by Y. S. Ywang, Technical Report No. 165, October 1983.

Participating Scientific Personnel

J. R. East
G. I. Haddad
M. Herman
Y. S. Hwang   Received Ph.D. in 1983
M. Majewski
C. K. Pao   Received Ph.D. in 1985
D. F. Peterson

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER Final Report ARO 18619.2-EL	2. GOVT ACCESSION NO. AD-A161 611 N/A	3. RECIPIENT'S CATALOG NUMBER N/A
4. TITLE (and Subtitle) HARMONIC POWER GENERATION OF IMPATT DIODES		5. TYPE OF REPORT & PERIOD COVERED Final Report 3/15/82-9/30/85
		6. PERFORMING ORG. REPORT NUMBER Technical Report No. 174
7. AUTHOR(s) C. K. Pao		8. CONTRACT OR GRANT NUMBER(s) DAAG29-82-K-0083
9. PERFORMING ORGANIZATION NAME AND ADDRESS The University of Michigan Solid-State Electronics Laboratory Ann Arbor, MI 48109-1109		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 18619-EL
11. CONTROLLING OFFICE NAME AND ADDRESS U. S. Army Research Office Post Office Box 12211 Research Triangle Park, NC 27709		12. REPORT DATE September 1985
		13. NUMBER OF PAGES 316
14. MONITORING AGENCY NAME & ADDRESS(If different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

NA

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Harmonic power generation	Si single-drift uniform diodes
Double-drift IMPATT diodes	pin diode structures
Drift-diffusion model	Three-frequency operation
Depletion-layer modulation	GaAs double-Read diode
GaAs uniform diode	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The harmonic power generation capability of IMPATT diodes is investigated
theoretically and experimentally. The existing computer simulation program for
IMPATT diodes, employing the drift-diffusion model, is used to investigate four
different conventional double-drift IMPATT diodes operated in the active mode
and three pin diodes with different lengths operated in the passive mode at a
fundamental frequency of 23 GHz. For conventional IMPATT diodes, the depletion-
layer modulation effect, which strongly depends on the diode doping structure,
is essential for harmonic power generation. Because of the moderate dependence

20 Contd.

of the harmonic current on the terminal RF voltage, the GaAs and Si uniform diodes seem to be promising devices for harmonic power generation. The GaAs uniform diode can achieve the highest third-harmonic efficiency, of the order of 4.1 percent, while the Si uniform diode can achieve the highest third-harmonic power of the order of 1.116 W.

In the case of pin diode structures, the device length determines the device RF power performance since it determines the space-charge and transit-time effects, both of which in turn affect the build-up and fall-off of the induced current. The optimum device length for achieving the highest third-harmonic power is approximately 0.827 μm. However, over 100-percent conversion of efficiency from the fundamental input power to the third-harmonic output power can be achieved.

An analytic model for three-frequency operation, without considering the depletion-layer modulation effect, was developed to investigate the GaAs double-Read diode. The calculated results showed that the third-harmonic power is low and the presence of the diode series resistance significantly decreases it.

Several waveguide circuits were designed for measurement of the RF power of GaAs double-Read diodes and Si single-drift uniform diodes. The best measured RF power levels for the GaAs diodes are 175 mW at 22.58 GHz, 2 mW at 45.59 GHz and 17 μW at 67.69 GHz, and those for the Si diodes are 15 mW at 32.43 GHz, 0.17 mW at 64.95 GHz and 2.2 μW at the third-harmonic frequency.

END

FILMED

1-86

DTIC